

R61505W

262,144-color, 240RGB x 320-dot Graphics Liquid Crystal Controller Driver for Amorphous-Silicon TFT Panel

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Description

The R61505W is a single-chip liquid crystal controller driver LSI for a-Si TFT panel, comprising frame memory for a maximum 240RGB x 320-dot graphics display, source driver, gate driver and power supply circuit. For efficient data transfer, the R61505W supports high-speed interface via 8-/9-/16-/18-bit ports as system interface to the host processor. The R61505W supports also RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and DB[17:0]) to display moving images.

The power supply circuit incorporates step-up circuits and voltage follower circuits to voltage levels to drive TFT liquid crystal panel.

The R61505W's power management functions i.e. 8-color display, the deep standby mode and so on make this LSI an ideal driver for the medium or small sized portable devices with color display systems such as digital cellular phones or small PDAs, where long battery life is a major concern.

Features

- A single-chip controller driver incorporating a gate circuit and a power supply circuit for a maximum 240RGB x 320-dot graphics display on amorphous TFT panel in 262,144 colors
- System interface
 - High-speed interfaces via 8-/9-/16-/18-bit parallel ports
 - Clock synchronous serial interface
- Moving picture display interface ^{Note}
 - 16-/18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and DB[17:0])
 - VSYNC interface (System interface + VSYNC)
 - FMARK interface (System interface + FMARK)
- Window address function to specify a rectangular area in the internal frame memory to write data
- Write data within a rectangular area in the internal frame memory via moving picture interface
 - Reduce data transfer by specifying the area in the frame memory to rewrite data
 - Enable displaying the data in the still picture frame memory area with a moving picture simultaneously
- Abundant color display and drawing functions
 - Programmable γ -correction function for 262,144-color display
 - Partial display function
- Low -power consumption architecture (enables to supply power directly to interface I/O)
 - Deep standby function
 - 8-color display function
 - Input power supply voltages: IOVCC (power supply for interface I/O)
VCC (power supply for logic regulator)
VCI (power supply for liquid crystal analog circuit)
- Incorporates a liquid crystal drive power supply circuit
 - Source driver liquid crystal drive/VCOM power supply: DDVDH, VREG1OUT, VCL, VCI
 - Gate drive power supply: VGH, VGL
 - VCOM drive (VCOM power supply): VCOMH
VCOML
- Liquid crystal power supply startup sequencer
- TFT storage capacitance: Cst only (common VCOM formula)
- 172,800-byte internal frame memory
- Internal 720-channel source driver and 320-channel gate driver
- Single-chip solution for COG module with the arrangement of gate circuits on both sides of the glass substrate
- Internal NVM: User identification code, 8 bits, VCOM level adjustment, 7 bits x 2 sets. Deleting data is guaranteed up to 5 times. Write/erase sequencer and write/erase power supply circuit are supported.
- Internal reference voltage to generate VREG1OUT

Note: Patent of moving picture display interface is granted.

United States Patent No. 7,176,870

Japanese Patent No. 3,826,159

Korean Patent No.747,636

Power Supply Specifications

Table 1

| No. | Item | R61505W | |
|-----|---------------------------------|--|--|
| 1 | TFT data lines | 720 | |
| 2 | TFT gate lines | 320 | |
| 3 | TFT display storage capacitance | Cst only (Common VCOM formula) | |
| 4 | Liquid crystal drive output | S1~S720 | Grayscale levels V0 ~ V63 |
| | | G1~320 | VGH-VGL |
| | | VCOM | VCOMH=3.0 ~ (DDVDH-0.5)V VCOML=(VCL+0.5) ~ 0V Amplitude between VCOMH and VCOML=max. 6V Change VCOMH with either electronic volume or from VCOMR Change VCOMH-VCOML amplitude with electronic volume |
| 5 | Input voltage | IOVCC (interface voltage) | 1.65V ~ 3.3V Power supply to IM0-3, RESETX, DB[17:0], RDX, SDI, SDO, WRX/SCL, RS, CSX, VSYNC, HSYNC, DOTCLK, ENABLE, FMARK Connect to VCC and VCI on the FPC when the electrical potentials are the same. |
| | | VCC (logic regulator power supply) | 2.5V ~ 3.3V Connect to IOVCC and VCI on the FPC when the electrical potentials are the same. |
| | | VCI (liquid crystal drive power supply voltage) | 2.5V ~ 3.3V Connect to IOVCC and VCC on the FPC when the electrical potentials are the same. |
| 6 | Liquid crystal drive voltages | DDVDH | 4.5V ~ 6.0V |
| | | VGH | 10.0V ~ 18.0V |
| | | VGL | -4.5V ~ -13.5V |
| | | VGH-VGL | Max. 28.0V |
| | | VCL | -1.9V ~ -3.0V |
| | | VCI-VCL | Max. 6.0V |
| 7 | Internal step-up circuits | DDVDH | VCI1 x 2 |
| | | VGH | VCI1 x 5, x 6 |
| | | VGL | VCI1 x -3, x -4, x -5 |
| | | VCL | VCI1 x -1 |

Differences between R61505V and R61505W

Table 2 Functions

| | | R61505V | R61505W |
|------------------|-----------------------------|---|---|
| FRC | | 64 grayscale output, without FRC | ← |
| RGB I/F | | 16/18 bits | ← |
| Partial display | | 1 image | ← |
| Sequencer | | Fully automatic | ← |
| Gamma correction | | 100 bits | ← |
| VCM | | 7 bit s | ← |
| DDVDH setting | | VCI1 x 2 | ← |
| VGH setting | | VCI1 x 5, 6 | ← |
| VGL setting | | VCI1 x -3, -4, -5 | ← |
| VCL setting | | VCI1 x -1 | ← |
| Serial interface | | 1 chip address only | ← |
| NVM | Erase | Erasable | ← |
| | Write/Erase sequencer | Manual | Automatic |
| | Write/Erase voltage | External power supply | Power supply circuit supported |
| | Write/Erase verify function | Not supported | Supported |
| | NVAD bit assignment | NVAD = 0 NVDAT[15]=VCMSEL NVDAT[14:8] = VCM1[6:0] NVDAT[6:0] = VCM2[6:0] | NVAD = 0 NVDAT[15]=VCMSEL NVDAT[14:8] = VCM2[6:0] NVDAT[6:0] = VCM1[6:0] |
| | | NVAD = 1 NVDAT[11:8] = UID1[3:0] | NVAD = 1 NVDAT[7:0] = UID1[7:0] |

Block Diagram

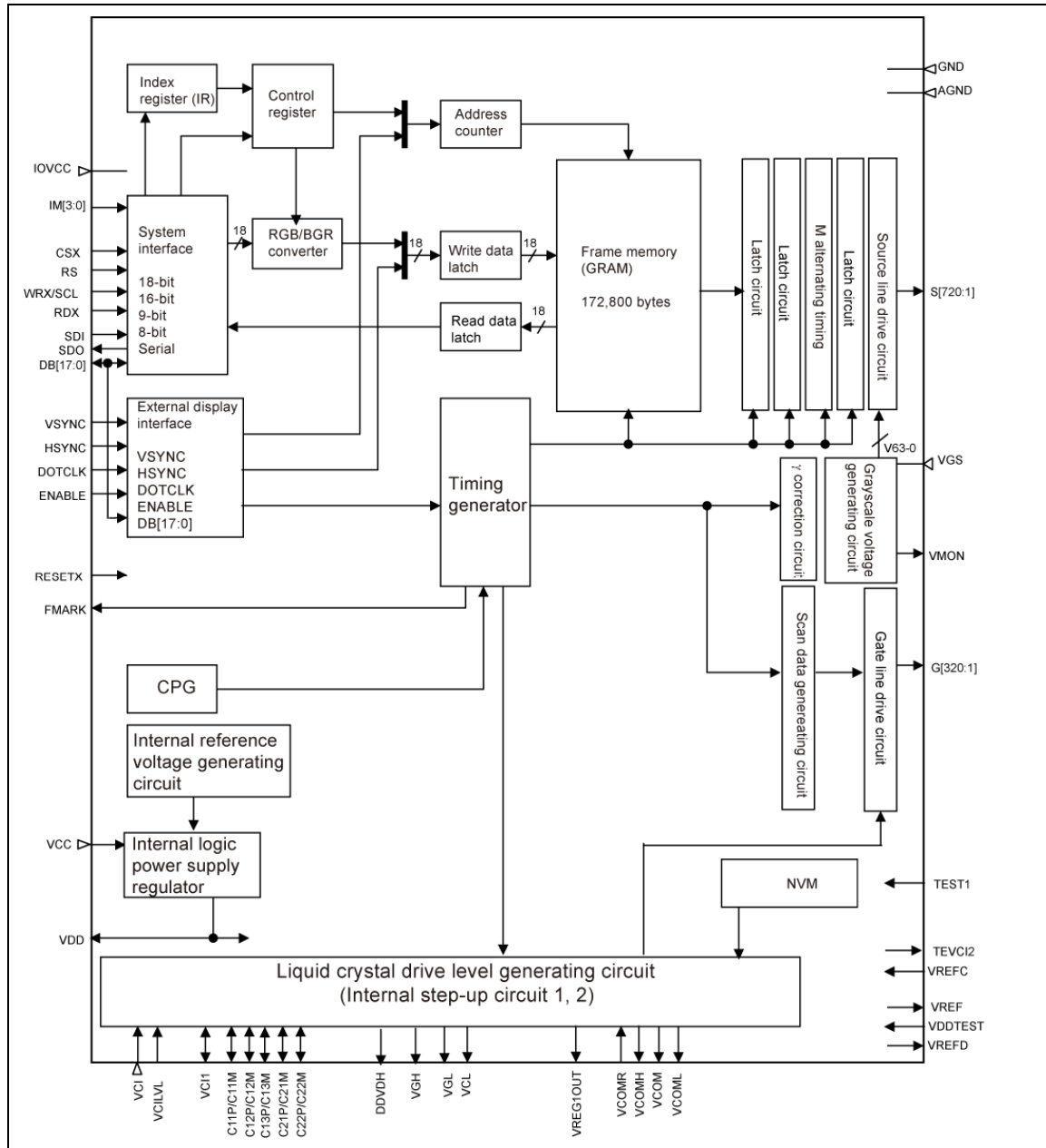


Figure 1

Block Function

1. System Interface

The R61505W supports 80-system high-speed interface via 8-/9-/16-/18-bit parallel ports and a clock synchronous serial interface. The interface is selected by setting the IM[3:0] pins.

The R61505W has a 16-bit index register (IR), an 18-bit write data register (WDR), and an 18-bit read data register (RDR). The IR is the register to store index information from control register and internal frame memory. The WDR is the register to temporarily store data to be written to control register and internal frame memory. The RDR is the register to temporarily store the data read from the frame memory. The data from the host processor to be written to the internal frame memory is first written to the WDR and then automatically written to the internal frame memory in internal operation. The data is read via RDR from the internal frame memory. Therefore, invalid data is sent to the data bus when the R61505W performs the first read operation from the internal frame memory. Valid data is read out when the R61505W performs the second and subsequent read operation.

The instruction execution time except that of starting oscillation takes 0 clock cycle to allow writing instructions consecutively.

Table 3 Register Selection (80-system 8-/9-/16-/18-bit Parallel Interface)

| WRX | RDX | RS | Function |
|-----|-----|----|--|
| 0 | 1 | 0 | Write index to IR |
| 1 | 0 | 0 | Setting disabled |
| 0 | 1 | 1 | Write to control register or internal frame memory via WDR |
| 1 | 0 | 1 | Read from internal frame memory and register via RDR |

Table 4 Register Selection (Clock Synchronous Serial Interface)

| Start byte | | |
|------------|----|--|
| RW | RS | Function |
| 0 | 0 | Write index to IR |
| 1 | 0 | Setting disabled |
| 0 | 1 | Write to control register or internal frame memory via WDR |
| 1 | 1 | Read from internal frame memory and register via RDR |

Table 5

| IM3 | IM2 | IM1 | IM0 | System interface | DB pins | Frame memory write data | Instruction write transfer |
|-----|-----|-----|-----|------------------------------------|-----------------------|---|--|
| 0 | 0 | 0 | 0 | Setting disabled | - | - | - |
| 0 | 0 | 0 | 1 | Setting disabled | - | - | - |
| 0 | 0 | 1 | 0 | 80-system 16-bit interface | DB[17:10], DB[8:1] | Single transfer (16 bits) 2 transfers (1 st : 2 bits, 2 nd : 16 bits) 2 transfers (1 st : 16 bits, 2 nd : 2 bits) | Single transfer (16 bits) |
| 0 | 0 | 1 | 1 | 80-system 8-bit interface | DB[17:10] | 2 transfers (1 st : 8 bits, 2 nd : 8 bits) 3 transfers (1 st : 6 bits, 2 nd : 6 bits, 3 rd : 6 bits) | 2 transfers (1 st : 8 bits, 2 nd : 8 bits) |
| 0 | 1 | 0 | 0 | Clock synchronous serial interface | - (SDI, SDO) | 2 transfers (1 st : 8 bits, 2 nd : 8 bits) | 2 transfers (1 st : 8 bits, 2 nd : 8 bits) |
| 0 | 1 | 0 | 1 | Setting disabled | - | - | - |
| 0 | 1 | 1 | 0 | Setting disabled | - | - | - |
| 0 | 1 | 1 | 1 | Setting disabled | - | - | - |
| 1 | 0 | 0 | 0 | Setting disabled | - | - | - |
| 1 | 0 | 0 | 1 | Setting disabled | - | - | - |
| 1 | 0 | 1 | 0 | 80-system 18-bit interface | DB[17:10] | Single transfer (18 bits) | Single transfer (16 bits) |
| 1 | 0 | 1 | 1 | 80-system 9-bit interface | DB[17:9] | 2 transfers (1 st : 9 bits, 2 nd : 9 bits) | 2 transfers (1 st : 8 bits, 2 nd : 8 bits) |
| 1 | 1 | 0 | 0 | Setting disabled | - | - | - |
| 1 | 1 | 0 | 1 | Setting disabled | - | - | - |
| 1 | 1 | 1 | 0 | Setting disabled | - | - | - |
| 1 | 1 | 1 | 1 | Setting disabled | - | - | - |

2. External Display Interface (RGB and VSYNC Interfaces)

The R61505W supports RGB interface and VSYNC interface as the external interface to display moving picture. When the RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface operation, data (DB[17:0]) is written in synchronization with these signals when the polarity of enable signal (ENABLE) allows write operation in order to prevent flicker while updating display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, which synchronizes the display operation with the VSYNC signal. The display data is written to the internal frame memory via system interface. When writing data via VSYNC interface, there are constraints in speed and method in writing data to the internal frame memory. For details, see the “VSYNC interface” section.

The R61505W allows switching interface by instruction according to the display, i.e. still and/or moving picture(s) in order to transfer data only when the data is updated and thereby reduce the data transfer and power consumption for moving picture display.

3. Address Counter (AC)

The address counter (AC) gives an address to the internal frame memory. When the index of the register to set a frame memory address in the AC is written to the IR, the address information is sent from the IR to the AC. As the R61505W writes data to the internal frame memory, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only within the rectangular area specified in the frame memory.

4. Frame Memory

The frame memory is graphics frame memory, which can store bit-pattern data of 172,800 (240RGB x 320 (dots) x 18(bits)) bytes at maximum, using 18 bits per pixel.

5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltages according to the grayscale data in the γ -correction registers to enable 262,144-color display. For details, see the γ -Correction Register section.

6. Liquid Crystal Drive Power Supply Circuit

The liquid crystal drive power supply circuit generates DDVDH, VGH, VGL and VCOM levels to drive liquid crystal.

7. Timing Generator

The timing generator generates a timing signal for the operation of internal circuit such as the internal frame memory. The timing signal for display operation such as frame memory read operation and the timing signal for internal operation such as frame memory access from the HOST PROCESSOR are generated separately in order to avoid mutual interference.

8. Oscillator (OSC)

Internal oscillator generates clock signal used to operate the R61505W.

The R61505W generates the internal oscillation clock using internal oscillator. Adjusting the frequency by external resistance is impossible. Adjust the oscillation frequency and line numbers by frame frequency adjustment function. During the deep standby mode, internal oscillation halts to reduce power consumption. See "Oscillator" for details.

9. Liquid Crystal Driver Circuit

The liquid crystal driver circuit of the R61505W consists of a 720-output source driver (S[720:1]) and a 320-output gate driver (G[320:1]). The display pattern data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver

can be changed by setting the SS bit and the shift direction of gate output from the gate driver can be changed by setting the GS bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

10. Internal Logic Power Supply Regulator

The internal logic power supply regulator generates internal logic power supply VDD.

Pin Function

Table 6 Interface Pins

| Signal | I/O | Connect to | Function | When not in use | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|-----|----------------|--|------------------|-----|-----|------------------------------------|-----------------------|--------------------------------------|--------|---|---|---|---|------------------|---|---|---|---|---|---|------------------|---|---|---|---|---|---|----------------------------|-----------------------|--------------------------------------|---|---|---|---|---------------------------|-----------|--------------------------------------|---|---|---|---|------------------------------------|---|--------|---|---|---|---|------------------|---|---|---|---|---|---|------------------|---|---|---|---|---|---|------------------|---|---|---|---|---|---|------------------|---|---|---|---|---|---|------------------|---|---|---|---|---|---|----------------------------|----------|---------|---|---|---|---|---------------------------|----------|---------|---|---|---|---|------------------|---|---|---|---|---|---|------------------|---|---|---|---|---|---|------------------|---|---|---|---|---|---|------------------|---|---|--|
| IM3-0 | I | GND or IOVCC | Select a mode to interface to host processor. (Amplitude: IOVCC ~ GND) | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | <table border="1"> <thead> <tr> <th>IM3</th> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>Interface Mode</th> <th>DB Pin</th> <th>Colors</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>80-system 16-bit interface</td> <td>DB[17:10], DB[8:1]</td> <td>262,144 <small>see Note 1</small></td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>80-system 8-bit interface</td> <td>DB[17:10]</td> <td>262,144 <small>see Note 2</small></td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>Clock synchronous serial interface</td> <td>-</td> <td>65,536</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>80-system 18-bit interface</td> <td>DB[17:0]</td> <td>262,144</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>80-system 9-bit interface</td> <td>DB[17:9]</td> <td>262,144</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> </tbody> </table> | IM3 | IM2 | IM1 | IM0 | Interface Mode | DB Pin | Colors | 0 | 0 | 0 | 0 | Setting disabled | - | - | 0 | 0 | 0 | 1 | Setting disabled | - | - | 0 | 0 | 1 | 0 | 80-system 16-bit interface | DB[17:10], DB[8:1] | 262,144 <small>see Note 1</small> | 0 | 0 | 1 | 1 | 80-system 8-bit interface | DB[17:10] | 262,144 <small>see Note 2</small> | 0 | 1 | 0 | 0 | Clock synchronous serial interface | - | 65,536 | 0 | 1 | 0 | 1 | Setting disabled | - | - | 0 | 1 | 1 | 0 | Setting disabled | - | - | 0 | 1 | 1 | 1 | Setting disabled | - | - | 1 | 0 | 0 | 0 | Setting disabled | - | - | 1 | 0 | 0 | 1 | Setting disabled | - | - | 1 | 0 | 1 | 0 | 80-system 18-bit interface | DB[17:0] | 262,144 | 1 | 0 | 1 | 1 | 80-system 9-bit interface | DB[17:9] | 262,144 | 1 | 1 | 0 | 0 | Setting disabled | - | - | 1 | 1 | 0 | 1 | Setting disabled | - | - | 1 | 1 | 1 | 0 | Setting disabled | - | - | 1 | 1 | 1 | 1 | Setting disabled | - | - | |
| | | | IM3 | IM2 | IM1 | IM0 | Interface Mode | DB Pin | Colors | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 0 | 0 | 0 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 0 | 0 | 1 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 0 | 1 | 0 | 80-system 16-bit interface | DB[17:10], DB[8:1] | 262,144 <small>see Note 1</small> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 0 | 1 | 1 | 80-system 8-bit interface | DB[17:10] | 262,144 <small>see Note 2</small> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 1 | 0 | 0 | Clock synchronous serial interface | - | 65,536 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 1 | 0 | 1 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 1 | 1 | 0 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 1 | 1 | 1 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | 0 | 0 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | 0 | 1 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | 1 | 0 | 80-system 18-bit interface | DB[17:0] | 262,144 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | 1 | 1 | 80-system 9-bit interface | DB[17:9] | 262,144 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 1 | 0 | 0 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | Setting disabled | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Notes: 1. 65,536 colors in one transfer mode 2. 65,536 colors in two transfers mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CSX | I | Host processor | Chip select signal. Amplitude: IOVCC-GND Low: the R61505W is selected and accessible High: the R61505W is not selected and not accessible. | IOVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RS | I | Host processor | Register select signal. Amplitude: IOVCC-GND Low: select Index register High: select control register | IOVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| WRX/SCL | I | Host processor | Write strobe signal in 80-system bus interface operation and enables write operation when WRX is low. Synchronous clock signal (SCL) in serial interface operation. Amplitude: IOVCC-GND | IOVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RDX | I | Host processor | Read strobe signal in 80-system bus interface operation and enables read operation when RDX is low. Amplitude: IOVCC-GND | IOVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SDI | I | Host processor | Serial data input (SDI) pin in serial interface operation. The data is inputted on the rising edge of the SCL signal. Amplitude: IOVCC-GND | GND or IOVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SDO | O | Host processor | Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal. Amplitude: IOVCC-GND | Open | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Signal | I/O | Connect to | Function | When not in use |
|----------|-----|----------------|--|-----------------|
| DB[17:0] | I/O | Host processor | 18-bit parallel bi-directional data bus for 80-system interface operation (Amplitude: IOVCC-GND). 8-bit I/F: DB[17:10] are used. 9-bit I/F: DB[17:9] are used. 16-bit I/F: DB[17:10] and DB[8:1] are used. 18-bit I/F: DB[17:0] are used. 18-bit parallel bi-directional data bus for RGB interface operation (Amplitude: IOVCC-GND). 16-bit I/F: DB[17:13] and DB[11:1] are used. 18-bit I/F: DB[17:0] are used. | GND or IOVCC |
| ENABLE | I | Host processor | Data enable signal for RGB interface operation. (Amplitude: IOVCC-GND). Low: accessible (select) High: Not accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit. (Amplitude: IOVCC-GND). | GND or IOVCC |
| VSYNC | I | Host processor | Frame synchronous signal for RGB interface operation. Low active. (Amplitude: IOVCC-GND). | GND or IOVCC |
| HSYNC | I | Host processor | Line synchronous signal for RGB interface operation. Low active. (Amplitude: IOVCC-GND). | GND or IOVCC |
| DOTCLK | I | Host processor | Dot clock signal for RGB interface operation. The data input timing is on the rising edge of DOTCLK. (Amplitude: IOVCC-GND). | GND or IOVCC |
| FMARK | O | Host processor | Frame head pulse signal, which is used when writing data to the internal frame memory. (Amplitude: IOVCC-GND). | Open |

Table 7 Reset and Internal Oscillation Pins

| Signal | I/O | Connect to | Function | When not in use |
|--------|-----|------------------------------------|---|-----------------|
| RESETX | I | Host processor or external circuit | Reset signal. The R61505W is initialized when this signal is at low level. Make sure to execute a power-on reset when turning on power supply (Amplitude: IOVCC-GND). | - |

Table 8 Power Supply Pins

| Signal | I/O | Connect to | Function | When not in use |
|--------|-----|------------------------|--|-----------------|
| VCC | - | Power supply | Power supply to internal logic regulator circuit. | - |
| GND | - | Power supply | Internal logic GND. | - |
| VDD | O | Stabilizing capacitor | Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor. | - |
| IOVCC | - | Power supply | Power supply to the interface pins: RESETX, CSX, WRX, RDX, RS, DB[17:0], VSYNC, HSYNC, DOTCLK, ENABLE. In case of COG, connect to VCC on the FPC if IOVCC=VCC, to prevent noise. | - |
| AGND | - | Power supply | Analog GND (for logic regulator and liquid crystal power supply circuit). In case of COG, connect to GND on the FPC to prevent noise. | - |
| VCI | I | Power supply | Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply VCI. | - |
| VCILVL | I | Reference power supply | VCILVL must be at the same electrical potential as VCI. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise. | - |

Table 9 Step-up Circuit Pins

| Signal | I/O | Connect to | Function | When not in use |
|--|-----|----------------------------------|--|-----------------|
| VCI1 | I/O | Stabilizing capacitor | Reference voltage of step-up circuit 1. Define the voltage so that DDVDH, VGH and VGL do not exceed the ratings. | - |
| DDVDH | O | Stabilizing capacitor | Power supply for the source driver liquid crystal drive unit and VCOM drive which is generated from VCI1 and output from internal step-up circuit 1. The step-up factor is 2. Make sure to connect to stabilizing capacitor. | - |
| VGH | O | Stabilizing capacitor, LCD panel | Liquid crystal drive power supply which is generated from VCI1 and DDVDH and output from internal step-up circuit 2. The step-up factor is set by BT bit. Make sure to connect to stabilizing capacitor. | - |
| VGL | O | Stabilizing capacitor, LCD panel | Liquid crystal drive power supply which is generated from VCI1 and DDVDH and output from internal step-up circuit 2. The step-up factor is set by BT bit. Make sure to connect to stabilizing capacitor. | - |
| VCL | O | Stabilizing capacitor | VCOML drive power supply. Make sure to connect to stabilizing capacitor. | - |
| C11P, C11M C12P, C12M | I/O | Step-up capacitor | Capacitor connection pins for the step-up circuit 1. | - |
| C13P, C13M, C21P, C21M, C22P, C22M | I/O | Step-up capacitor | Capacitor connection pins for the step-up circuit 2. | - |

Table 10 LCD Drive Pins

| Signal | I/O | Connect to | Function | When not in use |
|-----------|-----|----------------------------|--|-----------------|
| VREG1 OUT | O | Stabilizing capacitor | Output voltage generated from the reference voltage (VCILVL or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Make sure to connect to a stabilizing capacitor when in use. | - |
| VCOM | O | TFT panel common electrode | Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting. | - |
| VCOMH | O | Stabilizing capacitor | The High level of VCOM amplitude. The output level can be adjusted by either external resistor (VCOMR) or electronic volume. Make sure to connect to stabilizing capacitor. | - |
| VCOML | O | Stabilizing capacitor | The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). Make sure to connect to stabilizing capacitor. | - |
| VCOMR | I | Variable resistor or open | Connect a variable resistor when adjusting the VCOMH level between VREG1OUT and GND. | Open |
| VGS | I | GND | Reference level for the grayscale voltage generating circuit. | - |
| S[720:1] | O | LCD | Liquid crystal application voltages. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the frame memory address h00000 is output from S1. When SS = 1, the data in the frame memory address h00000 is output from S720. | - |
| G[320:1] | O | LCD | Gate line output signals. VGH: gate line select level VGL: gate line non-select level | - |

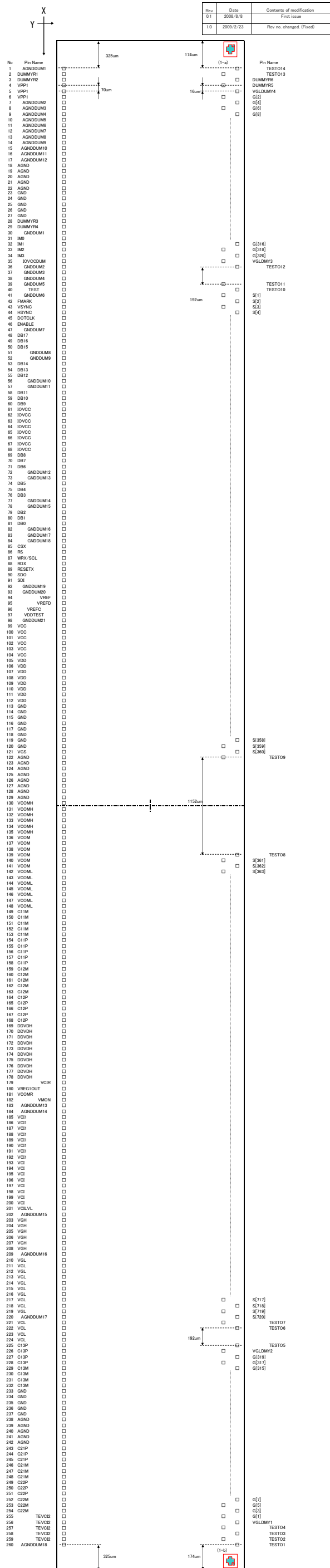
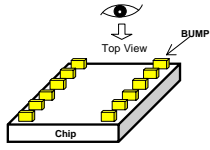
Table 11 Others (Test and Dummy Pins)

| Signal | I/O | Connect to | Function | When not in use |
|------------------------------------|-----|-------------------|--|-----------------|
| VREFC | I | GND | Test pin. Make sure to fix to the GND level. | - |
| VREFD | O | Open | Test pin. Leave open. | Open |
| VREF | O | Open | Test pin. Leave open. | Open |
| VDDTEST | I | GND | Test pin. Make sure to fix to the GND level. | - |
| VMON | O | Open | Test pin. Leave open. | Open |
| VCIR | O | Open | Test pin. Leave open. | Open |
| GNDDUM*, AGNDDUM*, IOVCCDUM* | O | - | Connect unused interface and test pins to these pins on the glass to fix voltage levels. Leave open when not used. | Open |
| DUMMYR* | - | - | Short-circuited within the chip for COG contact resistance measurement. DUMMYR pins are short-circuited as below: DUMMYR1 and DUMMYR6 DUMMYR2 and DUMMYR5 DUMMYR3 and DUMMYR4 | Open |
| VGLDMY* | O | Unused gate lines | Connect unused gate lines to fix the level at VGL. | Open |
| TEST* | I | GND | Test pin. Connect to GND. | GND |
| TEVCI2 | O | Open | Test pin. Leave open. | Open |
| VPP1 | I | AGND | Test pin. Connect to AGND. | AGND |

Patents of dummy pins used to fix pin to VCC or GND are granted as below:

PATENT ISSUED: United States Patent No. 6,323,930 No. 6,924,868
 Korean Patent No. 401,270
 Taiwanese Patent No. 175,413
 Japanese Patent No. 3,980,066

| Rev | Date | Contents of modification |
|-----|-----------|--------------------------|
| 0.1 | 2008/9/8 | First issue |
| 1.0 | 2009/2/23 | Rev no. changed. (Fixed) |



- No. Pin Name
- 1 AGNDUM1
- 2 DUMMYR1
- 3 DUMMYR2
- 4 VPP1
- 5 VPP1
- 6 VPP1
- 7 AGNDUM2
- 8 AGNDUM2
- 9 AGNDUM4
- 10 AGNDUM5
- 11 AGNDUM6
- 12 AGNDUM7
- 13 AGNDUM8
- 14 AGNDUM9
- 15 AGNDUM10
- 16 AGNDUM11
- 17 AGNDUM12
- 18 AGND
- 19 AGND
- 20 AGND
- 21 AGND
- 22 AGND
- 23 GND
- 24 GND
- 25 GND
- 26 GND
- 27 GND
- 28 DUMMYR3
- 29 DUMMYR4
- 30 GNDUM1
- 31 IM0
- 32 IM1
- 33 IM2
- 34 IM3
- 35 IOVCCUM
- 36 GNDUM2
- 37 GNDUM3
- 38 GNDUM4
- 39 GNDUM5
- 40 TEST
- 41 GNDUM6
- 42 FNARM
- 43 V2VNC
- 44 HSYNC
- 45 DDTCLK
- 46 ENABLE
- 47 GNDUM7
- 48 DB17
- 49 DB16
- 50 DB15
- 51 GNDUM8
- 52 GNDUM9
- 53 DB14
- 54 DB13
- 55 DB12
- 56 GNDUM10
- 57 GNDUM11
- 58 DB11
- 59 DB10
- 60 DB9
- 61 IOVCC
- 62 IOVCC
- 63 IOVCC
- 64 IOVCC
- 65 IOVCC
- 66 IOVCC
- 67 IOVCC
- 68 IOVCC
- 69 DB8
- 70 DB7
- 71 DB6
- 72 GNDUM12
- 73 GNDUM13
- 74 DB5
- 75 DB4
- 76 DB3
- 77 GNDUM14
- 78 GNDUM15
- 79 DB2
- 80 DB1
- 81 DB0
- 82 GNDUM16
- 83 GNDUM17
- 84 GNDUM18
- 85 CSX
- 86 RS
- 87 WRX SCL
- 88 RDX
- 89 RESETX
- 90 SDO
- 91 SCL
- 92 GNDUM19
- 93 GNDUM20
- 94 VREF
- 95 VREF2
- 96 VREFC
- 97 VDDTEST
- 98 GNDUM21
- 99 VCC
- 100 VCC
- 101 VCC
- 102 VCC
- 103 VCC
- 104 VCC
- 105 VCC
- 106 VDD
- 107 VDD
- 108 VDD
- 109 VDD
- 110 VDD
- 111 VDD
- 112 VDD
- 113 GND
- 114 GND
- 115 GND
- 116 GND
- 117 GND
- 118 GND
- 119 GND
- 120 GND
- 121 VGS
- 122 AGND
- 123 AGND
- 124 AGND
- 125 AGND
- 126 AGND
- 127 AGND
- 128 AGND
- 129 AGND
- 130 VCOMH
- 131 VCOMH
- 132 VCOMH
- 133 VCOMH
- 134 VCOMH
- 135 VCOMH
- 136 VCOM
- 137 VCOM
- 138 VCOM
- 139 VCOM
- 140 VCOM
- 141 VCOM
- 142 VCOML
- 143 VCOML
- 144 VCOML
- 145 VCOML
- 146 VCOML
- 147 VCOML
- 148 VCOML
- 149 VCOML
- 150 C11M
- 151 C11M
- 152 C11M
- 153 C11M
- 154 C11P
- 155 C11P
- 156 C11P
- 157 C11P
- 158 C11P
- 159 C12M
- 160 C12M
- 161 C12M
- 162 C12M
- 163 C12M
- 164 C12P
- 165 C12P
- 166 C12P
- 167 C12P
- 168 C12P
- 169 DDVDH
- 170 DDVDH
- 171 DDVDH
- 172 DDVDH
- 173 DDVDH
- 174 DDVDH
- 175 DDVDH
- 176 DDVDH
- 177 DDVDH
- 178 DDVDH
- 179 VGR
- 180 VREGIOUT
- 181 VCOMR
- 182 VCOM
- 183 AGNDUM13
- 184 AGNDUM14
- 185 VCI
- 186 VCI
- 187 VCI
- 188 VCI
- 189 VCI
- 190 VCI
- 191 VCI
- 192 VCI
- 193 VCI
- 194 VCI
- 195 VCI
- 196 VCI
- 197 VCI
- 198 VCI
- 199 VCI
- 200 VCI
- 201 VCLVL
- 202 AGNDUM15
- 203 VGH
- 204 VGH
- 205 VGH
- 206 VGH
- 207 VGH
- 208 VGH
- 209 AGNDUM16
- 210 VGL
- 211 VGL
- 212 VGL
- 213 VGL
- 214 VGL
- 215 VGL
- 216 VGL
- 217 VGL
- 218 VGL
- 219 VGL
- 220 AGNDUM17
- 221 VCL
- 222 VCL
- 223 VCL
- 224 C13P
- 225 C13P
- 226 C13P
- 227 C13P
- 228 C13M
- 229 C13M
- 230 C13M
- 231 C13M
- 232 C13M
- 233 GND
- 234 GND
- 235 GND
- 236 GND
- 237 GND
- 238 AGND
- 239 AGND
- 240 AGND
- 241 AGND
- 242 AGND
- 243 C21P
- 244 C21P
- 245 C21P
- 246 C21M
- 247 C21M
- 248 C21M
- 249 C21M
- 250 C22P
- 251 C22P
- 252 C22M
- 253 C22M
- 254 C22M
- 255 TEVCI
- 256 TEVCI
- 257 TEVCI
- 258 TEVCI
- 259 AGNDUM18

- Pin Name
- TEST014
- TEST013
- DUMMYR5
- VGLDMF4
- G(2)
- G(4)
- G(6)
- G(8)
- G(14)
- G(18)
- G(20)
- VGLDMF3
- TEST012
- TEST011
- TEST010
- S(1)
- S(2)
- S(3)
- S(4)
- S(36)
- S(38)
- S(36)
- TEST09
- TEST08
- S(361)
- S(362)
- S(363)
- S(71)
- S(74)
- S(78)
- S(20)
- TEST07
- TEST06
- TEST05
- VGLDMF2
- G(18)
- G(17)
- G(15)
- G(7)
- G(5)
- G(1)
- VGLDMF1
- TEST04
- TEST03
- TEST02
- TEST01

- Chip size: 18.78mm x 0.60mm
- Chip thickness: 280μm (typ.)
- Pad coordinates: Pad center
- Pad coordinates: Chip center

- Au bump size:
 1. 50μm x 50μm (I/O)
 2. 16μm x 85μm (Output to liquid crystal)
- Au bump pitch: See “Bump Arrangement”
- Au bump height: 12 μm

Table 12 Alignment Mark

| Alignment Mark shape | X | Y |
|----------------------|-------|-----|
| (1-a) | -9301 | 211 |
| (1-b) | 9301 | 211 |

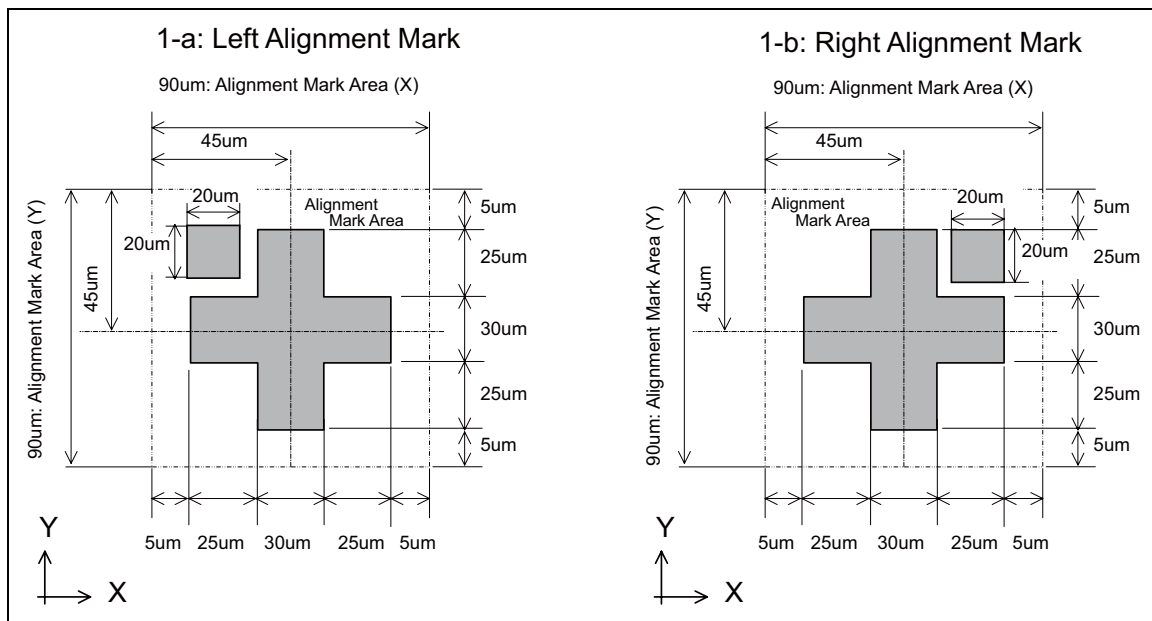


Figure 2 Alignment Mark

R61505W PAD Coordinates (unit: um) (No.1)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|-----------|----------|---------|
| 1 | AGNDDUM1 | -9065.00 | -226.20 |
| 2 | DUMMYR1 | -8995.00 | -226.20 |
| 3 | DUMMYR2 | -8925.00 | -226.20 |
| 4 | VPP1 | -8855.00 | -226.20 |
| 5 | VPP1 | -8785.00 | -226.20 |
| 6 | VPP1 | -8715.00 | -226.20 |
| 7 | AGNDDUM2 | -8645.00 | -226.20 |
| 8 | AGNDDUM3 | -8575.00 | -226.20 |
| 9 | AGNDDUM4 | -8505.00 | -226.20 |
| 10 | AGNDDUM5 | -8435.00 | -226.20 |
| 11 | AGNDDUM6 | -8365.00 | -226.20 |
| 12 | AGNDDUM7 | -8295.00 | -226.20 |
| 13 | AGNDDUM8 | -8225.00 | -226.20 |
| 14 | AGNDDUM9 | -8155.00 | -226.20 |
| 15 | AGNDDUM10 | -8085.00 | -226.20 |
| 16 | AGNDDUM11 | -8015.00 | -226.20 |
| 17 | AGNDDUM12 | -7945.00 | -226.20 |
| 18 | AGND | -7875.00 | -226.20 |
| 19 | AGND | -7805.00 | -226.20 |
| 20 | AGND | -7735.00 | -226.20 |
| 21 | AGND | -7665.00 | -226.20 |
| 22 | AGND | -7595.00 | -226.20 |
| 23 | GND | -7525.00 | -226.20 |
| 24 | GND | -7455.00 | -226.20 |
| 25 | GND | -7385.00 | -226.20 |
| 26 | GND | -7315.00 | -226.20 |
| 27 | GND | -7245.00 | -226.20 |
| 28 | DUMMYR3 | -7175.00 | -226.20 |
| 29 | DUMMYR4 | -7105.00 | -226.20 |
| 30 | GNDDUM1 | -7035.00 | -226.20 |
| 31 | IM0 | -6965.00 | -226.20 |
| 32 | IM1 | -6895.00 | -226.20 |
| 33 | IM2 | -6825.00 | -226.20 |
| 34 | IM3 | -6755.00 | -226.20 |
| 35 | IOVCCDUM | -6685.00 | -226.20 |
| 36 | GNDDUM2 | -6615.00 | -226.20 |
| 37 | GNDDUM3 | -6545.00 | -226.20 |
| 38 | GNDDUM4 | -6475.00 | -226.20 |
| 39 | GNDDUM5 | -6405.00 | -226.20 |
| 40 | TEST | -6335.00 | -226.20 |
| 41 | GNDDUM6 | -6265.00 | -226.20 |
| 42 | FMARK | -6195.00 | -226.20 |
| 43 | VSYN | -6125.00 | -226.20 |
| 44 | HSYN | -6055.00 | -226.20 |
| 45 | DOTCLK | -5985.00 | -226.20 |
| 46 | DE | -5915.00 | -226.20 |
| 47 | GNDDUM7 | -5845.00 | -226.20 |
| 48 | DB17 | -5775.00 | -226.20 |
| 49 | DB16 | -5705.00 | -226.20 |
| 50 | DB15 | -5635.00 | -226.20 |

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|---------|
| 51 | GNDDUM8 | -5565.00 | -226.20 |
| 52 | GNDDUM9 | -5495.00 | -226.20 |
| 53 | DB14 | -5425.00 | -226.20 |
| 54 | DB13 | -5355.00 | -226.20 |
| 55 | DB12 | -5285.00 | -226.20 |
| 56 | GNDDUM10 | -5215.00 | -226.20 |
| 57 | GNDDUM11 | -5145.00 | -226.20 |
| 58 | DB11 | -5075.00 | -226.20 |
| 59 | DB10 | -5005.00 | -226.20 |
| 60 | DB9 | -4935.00 | -226.20 |
| 61 | IOVCC | -4865.00 | -226.20 |
| 62 | IOVCC | -4795.00 | -226.20 |
| 63 | IOVCC | -4725.00 | -226.20 |
| 64 | IOVCC | -4655.00 | -226.20 |
| 65 | IOVCC | -4585.00 | -226.20 |
| 66 | IOVCC | -4515.00 | -226.20 |
| 67 | IOVCC | -4445.00 | -226.20 |
| 68 | IOVCC | -4375.00 | -226.20 |
| 69 | DB8 | -4305.00 | -226.20 |
| 70 | DB7 | -4235.00 | -226.20 |
| 71 | DB6 | -4165.00 | -226.20 |
| 72 | GNDDUM12 | -4095.00 | -226.20 |
| 73 | GNDDUM13 | -4025.00 | -226.20 |
| 74 | DB5 | -3955.00 | -226.20 |
| 75 | DB4 | -3885.00 | -226.20 |
| 76 | DB3 | -3815.00 | -226.20 |
| 77 | GNDDUM14 | -3745.00 | -226.20 |
| 78 | GNDDUM15 | -3675.00 | -226.20 |
| 79 | DB2 | -3605.00 | -226.20 |
| 80 | DB1 | -3535.00 | -226.20 |
| 81 | DB0 | -3465.00 | -226.20 |
| 82 | GNDDUM16 | -3395.00 | -226.20 |
| 83 | GNDDUM17 | -3325.00 | -226.20 |
| 84 | GNDDUM18 | -3255.00 | -226.20 |
| 85 | CSX | -3185.00 | -226.20 |
| 86 | RS | -3115.00 | -226.20 |
| 87 | WRX/SCL | -3045.00 | -226.20 |
| 88 | RDX | -2975.00 | -226.20 |
| 89 | RESETX | -2905.00 | -226.20 |
| 90 | SDO | -2835.00 | -226.20 |
| 91 | SDI | -2765.00 | -226.20 |
| 92 | GNDDUM19 | -2695.00 | -226.20 |
| 93 | GNDDUM20 | -2625.00 | -226.20 |
| 94 | VREF | -2555.00 | -226.20 |
| 95 | VREFD | -2485.00 | -226.20 |
| 96 | VREFC | -2415.00 | -226.20 |
| 97 | VDDTEST | -2345.00 | -226.20 |
| 98 | GNDDUM21 | -2275.00 | -226.20 |
| 99 | VCC | -2205.00 | -226.20 |
| 100 | VCC | -2135.00 | -226.20 |

R61505W PAD Coordinates (unit: um) (No.2)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|---------|
| 101 | VCC | -2065.00 | -226.20 |
| 102 | VCC | -1995.00 | -226.20 |
| 103 | VCC | -1925.00 | -226.20 |
| 104 | VCC | -1855.00 | -226.20 |
| 105 | VDD | -1785.00 | -226.20 |
| 106 | VDD | -1715.00 | -226.20 |
| 107 | VDD | -1645.00 | -226.20 |
| 108 | VDD | -1575.00 | -226.20 |
| 109 | VDD | -1505.00 | -226.20 |
| 110 | VDD | -1435.00 | -226.20 |
| 111 | VDD | -1365.00 | -226.20 |
| 112 | VDD | -1295.00 | -226.20 |
| 113 | GND | -1225.00 | -226.20 |
| 114 | GND | -1155.00 | -226.20 |
| 115 | GND | -1085.00 | -226.20 |
| 116 | GND | -1015.00 | -226.20 |
| 117 | GND | -945.00 | -226.20 |
| 118 | GND | -875.00 | -226.20 |
| 119 | GND | -805.00 | -226.20 |
| 120 | GND | -735.00 | -226.20 |
| 121 | VGS | -665.00 | -226.20 |
| 122 | AGND | -595.00 | -226.20 |
| 123 | AGND | -525.00 | -226.20 |
| 124 | AGND | -455.00 | -226.20 |
| 125 | AGND | -385.00 | -226.20 |
| 126 | AGND | -315.00 | -226.20 |
| 127 | AGND | -245.00 | -226.20 |
| 128 | AGND | -175.00 | -226.20 |
| 129 | AGND | -105.00 | -226.20 |
| 130 | VCOMH | -35.00 | -226.20 |
| 131 | VCOMH | 35.00 | -226.20 |
| 132 | VCOMH | 105.00 | -226.20 |
| 133 | VCOMH | 175.00 | -226.20 |
| 134 | VCOMH | 245.00 | -226.20 |
| 135 | VCOMH | 315.00 | -226.20 |
| 136 | VCOM | 385.00 | -226.20 |
| 137 | VCOM | 455.00 | -226.20 |
| 138 | VCOM | 525.00 | -226.20 |
| 139 | VCOM | 595.00 | -226.20 |
| 140 | VCOM | 665.00 | -226.20 |
| 141 | VCOM | 735.00 | -226.20 |
| 142 | VCOML | 805.00 | -226.20 |
| 143 | VCOML | 875.00 | -226.20 |
| 144 | VCOML | 945.00 | -226.20 |
| 145 | VCOML | 1015.00 | -226.20 |
| 146 | VCOML | 1085.00 | -226.20 |
| 147 | VCOML | 1155.00 | -226.20 |
| 148 | VCOML | 1225.00 | -226.20 |
| 149 | C11M | 1295.00 | -226.20 |
| 150 | C11M | 1365.00 | -226.20 |

| Pad No. | Pad Name | X | Y |
|---------|-----------|---------|---------|
| 151 | C11M | 1435.00 | -226.20 |
| 152 | C11M | 1505.00 | -226.20 |
| 153 | C11M | 1575.00 | -226.20 |
| 154 | C11P | 1645.00 | -226.20 |
| 155 | C11P | 1715.00 | -226.20 |
| 156 | C11P | 1785.00 | -226.20 |
| 157 | C11P | 1855.00 | -226.20 |
| 158 | C11P | 1925.00 | -226.20 |
| 159 | C12M | 1995.00 | -226.20 |
| 160 | C12M | 2065.00 | -226.20 |
| 161 | C12M | 2135.00 | -226.20 |
| 162 | C12M | 2205.00 | -226.20 |
| 163 | C12M | 2275.00 | -226.20 |
| 164 | C12P | 2345.00 | -226.20 |
| 165 | C12P | 2415.00 | -226.20 |
| 166 | C12P | 2485.00 | -226.20 |
| 167 | C12P | 2555.00 | -226.20 |
| 168 | C12P | 2625.00 | -226.20 |
| 169 | DDVDH | 2695.00 | -226.20 |
| 170 | DDVDH | 2765.00 | -226.20 |
| 171 | DDVDH | 2835.00 | -226.20 |
| 172 | DDVDH | 2905.00 | -226.20 |
| 173 | DDVDH | 2975.00 | -226.20 |
| 174 | DDVDH | 3045.00 | -226.20 |
| 175 | DDVDH | 3115.00 | -226.20 |
| 176 | DDVDH | 3185.00 | -226.20 |
| 177 | DDVDH | 3255.00 | -226.20 |
| 178 | DDVDH | 3325.00 | -226.20 |
| 179 | VCIR | 3395.00 | -226.20 |
| 180 | VREG1OUT | 3465.00 | -226.20 |
| 181 | VCOMR | 3535.00 | -226.20 |
| 182 | VMON | 3605.00 | -226.20 |
| 183 | AGNDDUM13 | 3675.00 | -226.20 |
| 184 | AGNDDUM14 | 3745.00 | -226.20 |
| 185 | VCI1 | 3815.00 | -226.20 |
| 186 | VCI1 | 3885.00 | -226.20 |
| 187 | VCI1 | 3955.00 | -226.20 |
| 188 | VCI1 | 4025.00 | -226.20 |
| 189 | VCI1 | 4095.00 | -226.20 |
| 190 | VCI1 | 4165.00 | -226.20 |
| 191 | VCI1 | 4235.00 | -226.20 |
| 192 | VCI1 | 4305.00 | -226.20 |
| 193 | VCI | 4375.00 | -226.20 |
| 194 | VCI | 4445.00 | -226.20 |
| 195 | VCI | 4515.00 | -226.20 |
| 196 | VCI | 4585.00 | -226.20 |
| 197 | VCI | 4655.00 | -226.20 |
| 198 | VCI | 4725.00 | -226.20 |
| 199 | VCI | 4795.00 | -226.20 |
| 200 | VCI | 4865.00 | -226.20 |

R61505W PAD Coordinates (unit: um) (No.3)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|-----------|---------|---------|
| 201 | VCILVL | 4935.00 | -226.20 |
| 202 | AGNDDUM15 | 5005.00 | -226.20 |
| 203 | VGH | 5075.00 | -226.20 |
| 204 | VGH | 5145.00 | -226.20 |
| 205 | VGH | 5215.00 | -226.20 |
| 206 | VGH | 5285.00 | -226.20 |
| 207 | VGH | 5355.00 | -226.20 |
| 208 | VGH | 5425.00 | -226.20 |
| 209 | AGNDDUM16 | 5495.00 | -226.20 |
| 210 | VGL | 5565.00 | -226.20 |
| 211 | VGL | 5635.00 | -226.20 |
| 212 | VGL | 5705.00 | -226.20 |
| 213 | VGL | 5775.00 | -226.20 |
| 214 | VGL | 5845.00 | -226.20 |
| 215 | VGL | 5915.00 | -226.20 |
| 216 | VGL | 5985.00 | -226.20 |
| 217 | VGL | 6055.00 | -226.20 |
| 218 | VGL | 6125.00 | -226.20 |
| 219 | VGL | 6195.00 | -226.20 |
| 220 | AGNDDUM17 | 6265.00 | -226.20 |
| 221 | VCL | 6335.00 | -226.20 |
| 222 | VCL | 6405.00 | -226.20 |
| 223 | VCL | 6475.00 | -226.20 |
| 224 | VCL | 6545.00 | -226.20 |
| 225 | C13P | 6615.00 | -226.20 |
| 226 | C13P | 6685.00 | -226.20 |
| 227 | C13P | 6755.00 | -226.20 |
| 228 | C13P | 6825.00 | -226.20 |
| 229 | C13M | 6895.00 | -226.20 |
| 230 | C13M | 6965.00 | -226.20 |
| 231 | C13M | 7035.00 | -226.20 |
| 232 | C13M | 7105.00 | -226.20 |
| 233 | GND | 7175.00 | -226.20 |
| 234 | GND | 7245.00 | -226.20 |
| 235 | GND | 7315.00 | -226.20 |
| 236 | GND | 7385.00 | -226.20 |
| 237 | GND | 7455.00 | -226.20 |
| 238 | AGND | 7525.00 | -226.20 |
| 239 | AGND | 7595.00 | -226.20 |
| 240 | AGND | 7665.00 | -226.20 |
| 241 | AGND | 7735.00 | -226.20 |
| 242 | AGND | 7805.00 | -226.20 |
| 243 | C21P | 7875.00 | -226.20 |
| 244 | C21P | 7945.00 | -226.20 |
| 245 | C21P | 8015.00 | -226.20 |
| 246 | C21M | 8085.00 | -226.20 |
| 247 | C21M | 8155.00 | -226.20 |
| 248 | C21M | 8225.00 | -226.20 |
| 249 | C22P | 8295.00 | -226.20 |
| 250 | C22P | 8365.00 | -226.20 |

| Pad No. | Pad Name | X | Y |
|---------|-----------|---------|---------|
| 251 | C22P | 8435.00 | -226.20 |
| 252 | C22M | 8505.00 | -226.20 |
| 253 | C22M | 8575.00 | -226.20 |
| 254 | C22M | 8645.00 | -226.20 |
| 255 | TEVCI2 | 8715.00 | -226.20 |
| 256 | TEVCI2 | 8785.00 | -226.20 |
| 257 | TEVCI2 | 8855.00 | -226.20 |
| 258 | TEVCI2 | 8925.00 | -226.20 |
| 259 | TEVCI2 | 8995.00 | -226.20 |
| 260 | AGNDDUM18 | 9065.00 | -226.20 |
| 261 | TESTO1 | 9216.00 | 213.50 |
| 262 | TESTO2 | 9200.00 | 109.50 |
| 263 | TESTO3 | 9184.00 | 213.50 |
| 264 | TESTO4 | 9168.00 | 109.50 |
| 265 | VGLDMY1 | 9152.00 | 213.50 |
| 266 | G<1> | 9136.00 | 109.50 |
| 267 | G<3> | 9120.00 | 213.50 |
| 268 | G<5> | 9104.00 | 109.50 |
| 269 | G<7> | 9088.00 | 213.50 |
| 270 | G<9> | 9072.00 | 109.50 |
| 271 | G<11> | 9056.00 | 213.50 |
| 272 | G<13> | 9040.00 | 109.50 |
| 273 | G<15> | 9024.00 | 213.50 |
| 274 | G<17> | 9008.00 | 109.50 |
| 275 | G<19> | 8992.00 | 213.50 |
| 276 | G<21> | 8976.00 | 109.50 |
| 277 | G<23> | 8960.00 | 213.50 |
| 278 | G<25> | 8944.00 | 109.50 |
| 279 | G<27> | 8928.00 | 213.50 |
| 280 | G<29> | 8912.00 | 109.50 |
| 281 | G<31> | 8896.00 | 213.50 |
| 282 | G<33> | 8880.00 | 109.50 |
| 283 | G<35> | 8864.00 | 213.50 |
| 284 | G<37> | 8848.00 | 109.50 |
| 285 | G<39> | 8832.00 | 213.50 |
| 286 | G<41> | 8816.00 | 109.50 |
| 287 | G<43> | 8800.00 | 213.50 |
| 288 | G<45> | 8784.00 | 109.50 |
| 289 | G<47> | 8768.00 | 213.50 |
| 290 | G<49> | 8752.00 | 109.50 |
| 291 | G<51> | 8736.00 | 213.50 |
| 292 | G<53> | 8720.00 | 109.50 |
| 293 | G<55> | 8704.00 | 213.50 |
| 294 | G<57> | 8688.00 | 109.50 |
| 295 | G<59> | 8672.00 | 213.50 |
| 296 | G<61> | 8656.00 | 109.50 |
| 297 | G<63> | 8640.00 | 213.50 |
| 298 | G<65> | 8624.00 | 109.50 |
| 299 | G<67> | 8608.00 | 213.50 |
| 300 | G<69> | 8592.00 | 109.50 |

R61505W PAD Coordinates (unit: um) (No.4)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|----------|---------|--------|
| 301 | G<71> | 8576.00 | 213.50 |
| 302 | G<73> | 8560.00 | 109.50 |
| 303 | G<75> | 8544.00 | 213.50 |
| 304 | G<77> | 8528.00 | 109.50 |
| 305 | G<79> | 8512.00 | 213.50 |
| 306 | G<81> | 8496.00 | 109.50 |
| 307 | G<83> | 8480.00 | 213.50 |
| 308 | G<85> | 8464.00 | 109.50 |
| 309 | G<87> | 8448.00 | 213.50 |
| 310 | G<89> | 8432.00 | 109.50 |
| 311 | G<91> | 8416.00 | 213.50 |
| 312 | G<93> | 8400.00 | 109.50 |
| 313 | G<95> | 8384.00 | 213.50 |
| 314 | G<97> | 8368.00 | 109.50 |
| 315 | G<99> | 8352.00 | 213.50 |
| 316 | G<101> | 8336.00 | 109.50 |
| 317 | G<103> | 8320.00 | 213.50 |
| 318 | G<105> | 8304.00 | 109.50 |
| 319 | G<107> | 8288.00 | 213.50 |
| 320 | G<109> | 8272.00 | 109.50 |
| 321 | G<111> | 8256.00 | 213.50 |
| 322 | G<113> | 8240.00 | 109.50 |
| 323 | G<115> | 8224.00 | 213.50 |
| 324 | G<117> | 8208.00 | 109.50 |
| 325 | G<119> | 8192.00 | 213.50 |
| 326 | G<121> | 8176.00 | 109.50 |
| 327 | G<123> | 8160.00 | 213.50 |
| 328 | G<125> | 8144.00 | 109.50 |
| 329 | G<127> | 8128.00 | 213.50 |
| 330 | G<129> | 8112.00 | 109.50 |
| 331 | G<131> | 8096.00 | 213.50 |
| 332 | G<133> | 8080.00 | 109.50 |
| 333 | G<135> | 8064.00 | 213.50 |
| 334 | G<137> | 8048.00 | 109.50 |
| 335 | G<139> | 8032.00 | 213.50 |
| 336 | G<141> | 8016.00 | 109.50 |
| 337 | G<143> | 8000.00 | 213.50 |
| 338 | G<145> | 7984.00 | 109.50 |
| 339 | G<147> | 7968.00 | 213.50 |
| 340 | G<149> | 7952.00 | 109.50 |
| 341 | G<151> | 7936.00 | 213.50 |
| 342 | G<153> | 7920.00 | 109.50 |
| 343 | G<155> | 7904.00 | 213.50 |
| 344 | G<157> | 7888.00 | 109.50 |
| 345 | G<159> | 7872.00 | 213.50 |
| 346 | G<161> | 7856.00 | 109.50 |
| 347 | G<163> | 7840.00 | 213.50 |
| 348 | G<165> | 7824.00 | 109.50 |
| 349 | G<167> | 7808.00 | 213.50 |
| 350 | G<169> | 7792.00 | 109.50 |

| Pad No. | Pad Name | X | Y |
|---------|----------|---------|--------|
| 351 | G<171> | 7776.00 | 213.50 |
| 352 | G<173> | 7760.00 | 109.50 |
| 353 | G<175> | 7744.00 | 213.50 |
| 354 | G<177> | 7728.00 | 109.50 |
| 355 | G<179> | 7712.00 | 213.50 |
| 356 | G<181> | 7696.00 | 109.50 |
| 357 | G<183> | 7680.00 | 213.50 |
| 358 | G<185> | 7664.00 | 109.50 |
| 359 | G<187> | 7648.00 | 213.50 |
| 360 | G<189> | 7632.00 | 109.50 |
| 361 | G<191> | 7616.00 | 213.50 |
| 362 | G<193> | 7600.00 | 109.50 |
| 363 | G<195> | 7584.00 | 213.50 |
| 364 | G<197> | 7568.00 | 109.50 |
| 365 | G<199> | 7552.00 | 213.50 |
| 366 | G<201> | 7536.00 | 109.50 |
| 367 | G<203> | 7520.00 | 213.50 |
| 368 | G<205> | 7504.00 | 109.50 |
| 369 | G<207> | 7488.00 | 213.50 |
| 370 | G<209> | 7472.00 | 109.50 |
| 371 | G<211> | 7456.00 | 213.50 |
| 372 | G<213> | 7440.00 | 109.50 |
| 373 | G<215> | 7424.00 | 213.50 |
| 374 | G<217> | 7408.00 | 109.50 |
| 375 | G<219> | 7392.00 | 213.50 |
| 376 | G<221> | 7376.00 | 109.50 |
| 377 | G<223> | 7360.00 | 213.50 |
| 378 | G<225> | 7344.00 | 109.50 |
| 379 | G<227> | 7328.00 | 213.50 |
| 380 | G<229> | 7312.00 | 109.50 |
| 381 | G<231> | 7296.00 | 213.50 |
| 382 | G<233> | 7280.00 | 109.50 |
| 383 | G<235> | 7264.00 | 213.50 |
| 384 | G<237> | 7248.00 | 109.50 |
| 385 | G<239> | 7232.00 | 213.50 |
| 386 | G<241> | 7216.00 | 109.50 |
| 387 | G<243> | 7200.00 | 213.50 |
| 388 | G<245> | 7184.00 | 109.50 |
| 389 | G<247> | 7168.00 | 213.50 |
| 390 | G<249> | 7152.00 | 109.50 |
| 391 | G<251> | 7136.00 | 213.50 |
| 392 | G<253> | 7120.00 | 109.50 |
| 393 | G<255> | 7104.00 | 213.50 |
| 394 | G<257> | 7088.00 | 109.50 |
| 395 | G<259> | 7072.00 | 213.50 |
| 396 | G<261> | 7056.00 | 109.50 |
| 397 | G<263> | 7040.00 | 213.50 |
| 398 | G<265> | 7024.00 | 109.50 |
| 399 | G<267> | 7008.00 | 213.50 |
| 400 | G<269> | 6992.00 | 109.50 |

R61505W PAD Coordinates (unit: um) (No.5)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|------------|---------|--------|
| 401 | G<271> | 6976.00 | 213.50 |
| 402 | G<273> | 6960.00 | 109.50 |
| 403 | G<275> | 6944.00 | 213.50 |
| 404 | G<277> | 6928.00 | 109.50 |
| 405 | G<279> | 6912.00 | 213.50 |
| 406 | G<281> | 6896.00 | 109.50 |
| 407 | G<283> | 6880.00 | 213.50 |
| 408 | G<285> | 6864.00 | 109.50 |
| 409 | G<287> | 6848.00 | 213.50 |
| 410 | G<289> | 6832.00 | 109.50 |
| 411 | G<291> | 6816.00 | 213.50 |
| 412 | G<293> | 6800.00 | 109.50 |
| 413 | G<295> | 6784.00 | 213.50 |
| 414 | G<297> | 6768.00 | 109.50 |
| 415 | G<299> | 6752.00 | 213.50 |
| 416 | G<301> | 6736.00 | 109.50 |
| 417 | G<303> | 6720.00 | 213.50 |
| 418 | G<305> | 6704.00 | 109.50 |
| 419 | G<307> | 6688.00 | 213.50 |
| 420 | G<309> | 6672.00 | 109.50 |
| 421 | G<311> | 6656.00 | 213.50 |
| 422 | G<313> | 6640.00 | 109.50 |
| 423 | G<315> | 6624.00 | 213.50 |
| 424 | G<317> | 6608.00 | 109.50 |
| 425 | G<319> | 6592.00 | 213.50 |
| 426 | VGLDMY2 | 6576.00 | 109.50 |
| 427 | TESTO5 | 6560.00 | 213.50 |
| 428 | TESTO6 | 6368.00 | 213.50 |
| 429 | TESTO7 | 6352.00 | 109.50 |
| 430 | S_PIN<720> | 6336.00 | 213.50 |
| 431 | S_PIN<719> | 6320.00 | 109.50 |
| 432 | S_PIN<718> | 6304.00 | 213.50 |
| 433 | S_PIN<717> | 6288.00 | 109.50 |
| 434 | S_PIN<716> | 6272.00 | 213.50 |
| 435 | S_PIN<715> | 6256.00 | 109.50 |
| 436 | S_PIN<714> | 6240.00 | 213.50 |
| 437 | S_PIN<713> | 6224.00 | 109.50 |
| 438 | S_PIN<712> | 6208.00 | 213.50 |
| 439 | S_PIN<711> | 6192.00 | 109.50 |
| 440 | S_PIN<710> | 6176.00 | 213.50 |
| 441 | S_PIN<709> | 6160.00 | 109.50 |
| 442 | S_PIN<708> | 6144.00 | 213.50 |
| 443 | S_PIN<707> | 6128.00 | 109.50 |
| 444 | S_PIN<706> | 6112.00 | 213.50 |
| 445 | S_PIN<705> | 6096.00 | 109.50 |
| 446 | S_PIN<704> | 6080.00 | 213.50 |
| 447 | S_PIN<703> | 6064.00 | 109.50 |
| 448 | S_PIN<702> | 6048.00 | 213.50 |
| 449 | S_PIN<701> | 6032.00 | 109.50 |
| 450 | S_PIN<700> | 6016.00 | 213.50 |

| Pad No. | Pad Name | X | Y |
|---------|------------|---------|--------|
| 451 | S_PIN<699> | 6000.00 | 109.50 |
| 452 | S_PIN<698> | 5984.00 | 213.50 |
| 453 | S_PIN<697> | 5968.00 | 109.50 |
| 454 | S_PIN<696> | 5952.00 | 213.50 |
| 455 | S_PIN<695> | 5936.00 | 109.50 |
| 456 | S_PIN<694> | 5920.00 | 213.50 |
| 457 | S_PIN<693> | 5904.00 | 109.50 |
| 458 | S_PIN<692> | 5888.00 | 213.50 |
| 459 | S_PIN<691> | 5872.00 | 109.50 |
| 460 | S_PIN<690> | 5856.00 | 213.50 |
| 461 | S_PIN<689> | 5840.00 | 109.50 |
| 462 | S_PIN<688> | 5824.00 | 213.50 |
| 463 | S_PIN<687> | 5808.00 | 109.50 |
| 464 | S_PIN<686> | 5792.00 | 213.50 |
| 465 | S_PIN<685> | 5776.00 | 109.50 |
| 466 | S_PIN<684> | 5760.00 | 213.50 |
| 467 | S_PIN<683> | 5744.00 | 109.50 |
| 468 | S_PIN<682> | 5728.00 | 213.50 |
| 469 | S_PIN<681> | 5712.00 | 109.50 |
| 470 | S_PIN<680> | 5696.00 | 213.50 |
| 471 | S_PIN<679> | 5680.00 | 109.50 |
| 472 | S_PIN<678> | 5664.00 | 213.50 |
| 473 | S_PIN<677> | 5648.00 | 109.50 |
| 474 | S_PIN<676> | 5632.00 | 213.50 |
| 475 | S_PIN<675> | 5616.00 | 109.50 |
| 476 | S_PIN<674> | 5600.00 | 213.50 |
| 477 | S_PIN<673> | 5584.00 | 109.50 |
| 478 | S_PIN<672> | 5568.00 | 213.50 |
| 479 | S_PIN<671> | 5552.00 | 109.50 |
| 480 | S_PIN<670> | 5536.00 | 213.50 |
| 481 | S_PIN<669> | 5520.00 | 109.50 |
| 482 | S_PIN<668> | 5504.00 | 213.50 |
| 483 | S_PIN<667> | 5488.00 | 109.50 |
| 484 | S_PIN<666> | 5472.00 | 213.50 |
| 485 | S_PIN<665> | 5456.00 | 109.50 |
| 486 | S_PIN<664> | 5440.00 | 213.50 |
| 487 | S_PIN<663> | 5424.00 | 109.50 |
| 488 | S_PIN<662> | 5408.00 | 213.50 |
| 489 | S_PIN<661> | 5392.00 | 109.50 |
| 490 | S_PIN<660> | 5376.00 | 213.50 |
| 491 | S_PIN<659> | 5360.00 | 109.50 |
| 492 | S_PIN<658> | 5344.00 | 213.50 |
| 493 | S_PIN<657> | 5328.00 | 109.50 |
| 494 | S_PIN<656> | 5312.00 | 213.50 |
| 495 | S_PIN<655> | 5296.00 | 109.50 |
| 496 | S_PIN<654> | 5280.00 | 213.50 |
| 497 | S_PIN<653> | 5264.00 | 109.50 |
| 498 | S_PIN<652> | 5248.00 | 213.50 |
| 499 | S_PIN<651> | 5232.00 | 109.50 |
| 500 | S_PIN<650> | 5216.00 | 213.50 |

R61505W PAD Coordinates (unit: um) (No.6)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|------------|---------|--------|
| 501 | S_PIN<649> | 5200.00 | 109.50 |
| 502 | S_PIN<648> | 5184.00 | 213.50 |
| 503 | S_PIN<647> | 5168.00 | 109.50 |
| 504 | S_PIN<646> | 5152.00 | 213.50 |
| 505 | S_PIN<645> | 5136.00 | 109.50 |
| 506 | S_PIN<644> | 5120.00 | 213.50 |
| 507 | S_PIN<643> | 5104.00 | 109.50 |
| 508 | S_PIN<642> | 5088.00 | 213.50 |
| 509 | S_PIN<641> | 5072.00 | 109.50 |
| 510 | S_PIN<640> | 5056.00 | 213.50 |
| 511 | S_PIN<639> | 5040.00 | 109.50 |
| 512 | S_PIN<638> | 5024.00 | 213.50 |
| 513 | S_PIN<637> | 5008.00 | 109.50 |
| 514 | S_PIN<636> | 4992.00 | 213.50 |
| 515 | S_PIN<635> | 4976.00 | 109.50 |
| 516 | S_PIN<634> | 4960.00 | 213.50 |
| 517 | S_PIN<633> | 4944.00 | 109.50 |
| 518 | S_PIN<632> | 4928.00 | 213.50 |
| 519 | S_PIN<631> | 4912.00 | 109.50 |
| 520 | S_PIN<630> | 4896.00 | 213.50 |
| 521 | S_PIN<629> | 4880.00 | 109.50 |
| 522 | S_PIN<628> | 4864.00 | 213.50 |
| 523 | S_PIN<627> | 4848.00 | 109.50 |
| 524 | S_PIN<626> | 4832.00 | 213.50 |
| 525 | S_PIN<625> | 4816.00 | 109.50 |
| 526 | S_PIN<624> | 4800.00 | 213.50 |
| 527 | S_PIN<623> | 4784.00 | 109.50 |
| 528 | S_PIN<622> | 4768.00 | 213.50 |
| 529 | S_PIN<621> | 4752.00 | 109.50 |
| 530 | S_PIN<620> | 4736.00 | 213.50 |
| 531 | S_PIN<619> | 4720.00 | 109.50 |
| 532 | S_PIN<618> | 4704.00 | 213.50 |
| 533 | S_PIN<617> | 4688.00 | 109.50 |
| 534 | S_PIN<616> | 4672.00 | 213.50 |
| 535 | S_PIN<615> | 4656.00 | 109.50 |
| 536 | S_PIN<614> | 4640.00 | 213.50 |
| 537 | S_PIN<613> | 4624.00 | 109.50 |
| 538 | S_PIN<612> | 4608.00 | 213.50 |
| 539 | S_PIN<611> | 4592.00 | 109.50 |
| 540 | S_PIN<610> | 4576.00 | 213.50 |
| 541 | S_PIN<609> | 4560.00 | 109.50 |
| 542 | S_PIN<608> | 4544.00 | 213.50 |
| 543 | S_PIN<607> | 4528.00 | 109.50 |
| 544 | S_PIN<606> | 4512.00 | 213.50 |
| 545 | S_PIN<605> | 4496.00 | 109.50 |
| 546 | S_PIN<604> | 4480.00 | 213.50 |
| 547 | S_PIN<603> | 4464.00 | 109.50 |
| 548 | S_PIN<602> | 4448.00 | 213.50 |
| 549 | S_PIN<601> | 4432.00 | 109.50 |
| 550 | S_PIN<600> | 4416.00 | 213.50 |

| Pad No. | Pad Name | X | Y |
|---------|------------|---------|--------|
| 551 | S_PIN<599> | 4400.00 | 109.50 |
| 552 | S_PIN<598> | 4384.00 | 213.50 |
| 553 | S_PIN<597> | 4368.00 | 109.50 |
| 554 | S_PIN<596> | 4352.00 | 213.50 |
| 555 | S_PIN<595> | 4336.00 | 109.50 |
| 556 | S_PIN<594> | 4320.00 | 213.50 |
| 557 | S_PIN<593> | 4304.00 | 109.50 |
| 558 | S_PIN<592> | 4288.00 | 213.50 |
| 559 | S_PIN<591> | 4272.00 | 109.50 |
| 560 | S_PIN<590> | 4256.00 | 213.50 |
| 561 | S_PIN<589> | 4240.00 | 109.50 |
| 562 | S_PIN<588> | 4224.00 | 213.50 |
| 563 | S_PIN<587> | 4208.00 | 109.50 |
| 564 | S_PIN<586> | 4192.00 | 213.50 |
| 565 | S_PIN<585> | 4176.00 | 109.50 |
| 566 | S_PIN<584> | 4160.00 | 213.50 |
| 567 | S_PIN<583> | 4144.00 | 109.50 |
| 568 | S_PIN<582> | 4128.00 | 213.50 |
| 569 | S_PIN<581> | 4112.00 | 109.50 |
| 570 | S_PIN<580> | 4096.00 | 213.50 |
| 571 | S_PIN<579> | 4080.00 | 109.50 |
| 572 | S_PIN<578> | 4064.00 | 213.50 |
| 573 | S_PIN<577> | 4048.00 | 109.50 |
| 574 | S_PIN<576> | 4032.00 | 213.50 |
| 575 | S_PIN<575> | 4016.00 | 109.50 |
| 576 | S_PIN<574> | 4000.00 | 213.50 |
| 577 | S_PIN<573> | 3984.00 | 109.50 |
| 578 | S_PIN<572> | 3968.00 | 213.50 |
| 579 | S_PIN<571> | 3952.00 | 109.50 |
| 580 | S_PIN<570> | 3936.00 | 213.50 |
| 581 | S_PIN<569> | 3920.00 | 109.50 |
| 582 | S_PIN<568> | 3904.00 | 213.50 |
| 583 | S_PIN<567> | 3888.00 | 109.50 |
| 584 | S_PIN<566> | 3872.00 | 213.50 |
| 585 | S_PIN<565> | 3856.00 | 109.50 |
| 586 | S_PIN<564> | 3840.00 | 213.50 |
| 587 | S_PIN<563> | 3824.00 | 109.50 |
| 588 | S_PIN<562> | 3808.00 | 213.50 |
| 589 | S_PIN<561> | 3792.00 | 109.50 |
| 590 | S_PIN<560> | 3776.00 | 213.50 |
| 591 | S_PIN<559> | 3760.00 | 109.50 |
| 592 | S_PIN<558> | 3744.00 | 213.50 |
| 593 | S_PIN<557> | 3728.00 | 109.50 |
| 594 | S_PIN<556> | 3712.00 | 213.50 |
| 595 | S_PIN<555> | 3696.00 | 109.50 |
| 596 | S_PIN<554> | 3680.00 | 213.50 |
| 597 | S_PIN<553> | 3664.00 | 109.50 |
| 598 | S_PIN<552> | 3648.00 | 213.50 |
| 599 | S_PIN<551> | 3632.00 | 109.50 |
| 600 | S_PIN<550> | 3616.00 | 213.50 |

R61505W PAD Coordinates (unit: um) (No.7)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|------------|---------|--------|
| 601 | S_PIN<549> | 3600.00 | 109.50 |
| 602 | S_PIN<548> | 3584.00 | 213.50 |
| 603 | S_PIN<547> | 3568.00 | 109.50 |
| 604 | S_PIN<546> | 3552.00 | 213.50 |
| 605 | S_PIN<545> | 3536.00 | 109.50 |
| 606 | S_PIN<544> | 3520.00 | 213.50 |
| 607 | S_PIN<543> | 3504.00 | 109.50 |
| 608 | S_PIN<542> | 3488.00 | 213.50 |
| 609 | S_PIN<541> | 3472.00 | 109.50 |
| 610 | S_PIN<540> | 3456.00 | 213.50 |
| 611 | S_PIN<539> | 3440.00 | 109.50 |
| 612 | S_PIN<538> | 3424.00 | 213.50 |
| 613 | S_PIN<537> | 3408.00 | 109.50 |
| 614 | S_PIN<536> | 3392.00 | 213.50 |
| 615 | S_PIN<535> | 3376.00 | 109.50 |
| 616 | S_PIN<534> | 3360.00 | 213.50 |
| 617 | S_PIN<533> | 3344.00 | 109.50 |
| 618 | S_PIN<532> | 3328.00 | 213.50 |
| 619 | S_PIN<531> | 3312.00 | 109.50 |
| 620 | S_PIN<530> | 3296.00 | 213.50 |
| 621 | S_PIN<529> | 3280.00 | 109.50 |
| 622 | S_PIN<528> | 3264.00 | 213.50 |
| 623 | S_PIN<527> | 3248.00 | 109.50 |
| 624 | S_PIN<526> | 3232.00 | 213.50 |
| 625 | S_PIN<525> | 3216.00 | 109.50 |
| 626 | S_PIN<524> | 3200.00 | 213.50 |
| 627 | S_PIN<523> | 3184.00 | 109.50 |
| 628 | S_PIN<522> | 3168.00 | 213.50 |
| 629 | S_PIN<521> | 3152.00 | 109.50 |
| 630 | S_PIN<520> | 3136.00 | 213.50 |
| 631 | S_PIN<519> | 3120.00 | 109.50 |
| 632 | S_PIN<518> | 3104.00 | 213.50 |
| 633 | S_PIN<517> | 3088.00 | 109.50 |
| 634 | S_PIN<516> | 3072.00 | 213.50 |
| 635 | S_PIN<515> | 3056.00 | 109.50 |
| 636 | S_PIN<514> | 3040.00 | 213.50 |
| 637 | S_PIN<513> | 3024.00 | 109.50 |
| 638 | S_PIN<512> | 3008.00 | 213.50 |
| 639 | S_PIN<511> | 2992.00 | 109.50 |
| 640 | S_PIN<510> | 2976.00 | 213.50 |
| 641 | S_PIN<509> | 2960.00 | 109.50 |
| 642 | S_PIN<508> | 2944.00 | 213.50 |
| 643 | S_PIN<507> | 2928.00 | 109.50 |
| 644 | S_PIN<506> | 2912.00 | 213.50 |
| 645 | S_PIN<505> | 2896.00 | 109.50 |
| 646 | S_PIN<504> | 2880.00 | 213.50 |
| 647 | S_PIN<503> | 2864.00 | 109.50 |
| 648 | S_PIN<502> | 2848.00 | 213.50 |
| 649 | S_PIN<501> | 2832.00 | 109.50 |
| 650 | S_PIN<500> | 2816.00 | 213.50 |

| Pad No. | Pad Name | X | Y |
|---------|------------|---------|--------|
| 651 | S_PIN<499> | 2800.00 | 109.50 |
| 652 | S_PIN<498> | 2784.00 | 213.50 |
| 653 | S_PIN<497> | 2768.00 | 109.50 |
| 654 | S_PIN<496> | 2752.00 | 213.50 |
| 655 | S_PIN<495> | 2736.00 | 109.50 |
| 656 | S_PIN<494> | 2720.00 | 213.50 |
| 657 | S_PIN<493> | 2704.00 | 109.50 |
| 658 | S_PIN<492> | 2688.00 | 213.50 |
| 659 | S_PIN<491> | 2672.00 | 109.50 |
| 660 | S_PIN<490> | 2656.00 | 213.50 |
| 661 | S_PIN<489> | 2640.00 | 109.50 |
| 662 | S_PIN<488> | 2624.00 | 213.50 |
| 663 | S_PIN<487> | 2608.00 | 109.50 |
| 664 | S_PIN<486> | 2592.00 | 213.50 |
| 665 | S_PIN<485> | 2576.00 | 109.50 |
| 666 | S_PIN<484> | 2560.00 | 213.50 |
| 667 | S_PIN<483> | 2544.00 | 109.50 |
| 668 | S_PIN<482> | 2528.00 | 213.50 |
| 669 | S_PIN<481> | 2512.00 | 109.50 |
| 670 | S_PIN<480> | 2496.00 | 213.50 |
| 671 | S_PIN<479> | 2480.00 | 109.50 |
| 672 | S_PIN<478> | 2464.00 | 213.50 |
| 673 | S_PIN<477> | 2448.00 | 109.50 |
| 674 | S_PIN<476> | 2432.00 | 213.50 |
| 675 | S_PIN<475> | 2416.00 | 109.50 |
| 676 | S_PIN<474> | 2400.00 | 213.50 |
| 677 | S_PIN<473> | 2384.00 | 109.50 |
| 678 | S_PIN<472> | 2368.00 | 213.50 |
| 679 | S_PIN<471> | 2352.00 | 109.50 |
| 680 | S_PIN<470> | 2336.00 | 213.50 |
| 681 | S_PIN<469> | 2320.00 | 109.50 |
| 682 | S_PIN<468> | 2304.00 | 213.50 |
| 683 | S_PIN<467> | 2288.00 | 109.50 |
| 684 | S_PIN<466> | 2272.00 | 213.50 |
| 685 | S_PIN<465> | 2256.00 | 109.50 |
| 686 | S_PIN<464> | 2240.00 | 213.50 |
| 687 | S_PIN<463> | 2224.00 | 109.50 |
| 688 | S_PIN<462> | 2208.00 | 213.50 |
| 689 | S_PIN<461> | 2192.00 | 109.50 |
| 690 | S_PIN<460> | 2176.00 | 213.50 |
| 691 | S_PIN<459> | 2160.00 | 109.50 |
| 692 | S_PIN<458> | 2144.00 | 213.50 |
| 693 | S_PIN<457> | 2128.00 | 109.50 |
| 694 | S_PIN<456> | 2112.00 | 213.50 |
| 695 | S_PIN<455> | 2096.00 | 109.50 |
| 696 | S_PIN<454> | 2080.00 | 213.50 |
| 697 | S_PIN<453> | 2064.00 | 109.50 |
| 698 | S_PIN<452> | 2048.00 | 213.50 |
| 699 | S_PIN<451> | 2032.00 | 109.50 |
| 700 | S_PIN<450> | 2016.00 | 213.50 |

R61505W PAD Coordinates (unit: um) (No.8)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|------------|---------|--------|
| 701 | S_PIN<449> | 2000.00 | 109.50 |
| 702 | S_PIN<448> | 1984.00 | 213.50 |
| 703 | S_PIN<447> | 1968.00 | 109.50 |
| 704 | S_PIN<446> | 1952.00 | 213.50 |
| 705 | S_PIN<445> | 1936.00 | 109.50 |
| 706 | S_PIN<444> | 1920.00 | 213.50 |
| 707 | S_PIN<443> | 1904.00 | 109.50 |
| 708 | S_PIN<442> | 1888.00 | 213.50 |
| 709 | S_PIN<441> | 1872.00 | 109.50 |
| 710 | S_PIN<440> | 1856.00 | 213.50 |
| 711 | S_PIN<439> | 1840.00 | 109.50 |
| 712 | S_PIN<438> | 1824.00 | 213.50 |
| 713 | S_PIN<437> | 1808.00 | 109.50 |
| 714 | S_PIN<436> | 1792.00 | 213.50 |
| 715 | S_PIN<435> | 1776.00 | 109.50 |
| 716 | S_PIN<434> | 1760.00 | 213.50 |
| 717 | S_PIN<433> | 1744.00 | 109.50 |
| 718 | S_PIN<432> | 1728.00 | 213.50 |
| 719 | S_PIN<431> | 1712.00 | 109.50 |
| 720 | S_PIN<430> | 1696.00 | 213.50 |
| 721 | S_PIN<429> | 1680.00 | 109.50 |
| 722 | S_PIN<428> | 1664.00 | 213.50 |
| 723 | S_PIN<427> | 1648.00 | 109.50 |
| 724 | S_PIN<426> | 1632.00 | 213.50 |
| 725 | S_PIN<425> | 1616.00 | 109.50 |
| 726 | S_PIN<424> | 1600.00 | 213.50 |
| 727 | S_PIN<423> | 1584.00 | 109.50 |
| 728 | S_PIN<422> | 1568.00 | 213.50 |
| 729 | S_PIN<421> | 1552.00 | 109.50 |
| 730 | S_PIN<420> | 1536.00 | 213.50 |
| 731 | S_PIN<419> | 1520.00 | 109.50 |
| 732 | S_PIN<418> | 1504.00 | 213.50 |
| 733 | S_PIN<417> | 1488.00 | 109.50 |
| 734 | S_PIN<416> | 1472.00 | 213.50 |
| 735 | S_PIN<415> | 1456.00 | 109.50 |
| 736 | S_PIN<414> | 1440.00 | 213.50 |
| 737 | S_PIN<413> | 1424.00 | 109.50 |
| 738 | S_PIN<412> | 1408.00 | 213.50 |
| 739 | S_PIN<411> | 1392.00 | 109.50 |
| 740 | S_PIN<410> | 1376.00 | 213.50 |
| 741 | S_PIN<409> | 1360.00 | 109.50 |
| 742 | S_PIN<408> | 1344.00 | 213.50 |
| 743 | S_PIN<407> | 1328.00 | 109.50 |
| 744 | S_PIN<406> | 1312.00 | 213.50 |
| 745 | S_PIN<405> | 1296.00 | 109.50 |
| 746 | S_PIN<404> | 1280.00 | 213.50 |
| 747 | S_PIN<403> | 1264.00 | 109.50 |
| 748 | S_PIN<402> | 1248.00 | 213.50 |
| 749 | S_PIN<401> | 1232.00 | 109.50 |
| 750 | S_PIN<400> | 1216.00 | 213.50 |

| Pad No. | Pad Name | X | Y |
|---------|------------|---------|--------|
| 751 | S_PIN<399> | 1200.00 | 109.50 |
| 752 | S_PIN<398> | 1184.00 | 213.50 |
| 753 | S_PIN<397> | 1168.00 | 109.50 |
| 754 | S_PIN<396> | 1152.00 | 213.50 |
| 755 | S_PIN<395> | 1136.00 | 109.50 |
| 756 | S_PIN<394> | 1120.00 | 213.50 |
| 757 | S_PIN<393> | 1104.00 | 109.50 |
| 758 | S_PIN<392> | 1088.00 | 213.50 |
| 759 | S_PIN<391> | 1072.00 | 109.50 |
| 760 | S_PIN<390> | 1056.00 | 213.50 |
| 761 | S_PIN<389> | 1040.00 | 109.50 |
| 762 | S_PIN<388> | 1024.00 | 213.50 |
| 763 | S_PIN<387> | 1008.00 | 109.50 |
| 764 | S_PIN<386> | 992.00 | 213.50 |
| 765 | S_PIN<385> | 976.00 | 109.50 |
| 766 | S_PIN<384> | 960.00 | 213.50 |
| 767 | S_PIN<383> | 944.00 | 109.50 |
| 768 | S_PIN<382> | 928.00 | 213.50 |
| 769 | S_PIN<381> | 912.00 | 109.50 |
| 770 | S_PIN<380> | 896.00 | 213.50 |
| 771 | S_PIN<379> | 880.00 | 109.50 |
| 772 | S_PIN<378> | 864.00 | 213.50 |
| 773 | S_PIN<377> | 848.00 | 109.50 |
| 774 | S_PIN<376> | 832.00 | 213.50 |
| 775 | S_PIN<375> | 816.00 | 109.50 |
| 776 | S_PIN<374> | 800.00 | 213.50 |
| 777 | S_PIN<373> | 784.00 | 109.50 |
| 778 | S_PIN<372> | 768.00 | 213.50 |
| 779 | S_PIN<371> | 752.00 | 109.50 |
| 780 | S_PIN<370> | 736.00 | 213.50 |
| 781 | S_PIN<369> | 720.00 | 109.50 |
| 782 | S_PIN<368> | 704.00 | 213.50 |
| 783 | S_PIN<367> | 688.00 | 109.50 |
| 784 | S_PIN<366> | 672.00 | 213.50 |
| 785 | S_PIN<365> | 656.00 | 109.50 |
| 786 | S_PIN<364> | 640.00 | 213.50 |
| 787 | S_PIN<363> | 624.00 | 109.50 |
| 788 | S_PIN<362> | 608.00 | 213.50 |
| 789 | S_PIN<361> | 592.00 | 109.50 |
| 790 | TESTO8 | 576.00 | 213.50 |
| 791 | TESTO9 | -576.00 | 109.50 |
| 792 | S_PIN<360> | -592.00 | 213.50 |
| 793 | S_PIN<359> | -608.00 | 109.50 |
| 794 | S_PIN<358> | -624.00 | 213.50 |
| 795 | S_PIN<357> | -640.00 | 109.50 |
| 796 | S_PIN<356> | -656.00 | 213.50 |
| 797 | S_PIN<355> | -672.00 | 109.50 |
| 798 | S_PIN<354> | -688.00 | 213.50 |
| 799 | S_PIN<353> | -704.00 | 109.50 |
| 800 | S_PIN<352> | -720.00 | 213.50 |

R61505W PAD Coordinates (unit: um) (No.9)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|------------|----------|--------|
| 801 | S_PIN<351> | -736.00 | 109.50 |
| 802 | S_PIN<350> | -752.00 | 213.50 |
| 803 | S_PIN<349> | -768.00 | 109.50 |
| 804 | S_PIN<348> | -784.00 | 213.50 |
| 805 | S_PIN<347> | -800.00 | 109.50 |
| 806 | S_PIN<346> | -816.00 | 213.50 |
| 807 | S_PIN<345> | -832.00 | 109.50 |
| 808 | S_PIN<344> | -848.00 | 213.50 |
| 809 | S_PIN<343> | -864.00 | 109.50 |
| 810 | S_PIN<342> | -880.00 | 213.50 |
| 811 | S_PIN<341> | -896.00 | 109.50 |
| 812 | S_PIN<340> | -912.00 | 213.50 |
| 813 | S_PIN<339> | -928.00 | 109.50 |
| 814 | S_PIN<338> | -944.00 | 213.50 |
| 815 | S_PIN<337> | -960.00 | 109.50 |
| 816 | S_PIN<336> | -976.00 | 213.50 |
| 817 | S_PIN<335> | -992.00 | 109.50 |
| 818 | S_PIN<334> | -1008.00 | 213.50 |
| 819 | S_PIN<333> | -1024.00 | 109.50 |
| 820 | S_PIN<332> | -1040.00 | 213.50 |
| 821 | S_PIN<331> | -1056.00 | 109.50 |
| 822 | S_PIN<330> | -1072.00 | 213.50 |
| 823 | S_PIN<329> | -1088.00 | 109.50 |
| 824 | S_PIN<328> | -1104.00 | 213.50 |
| 825 | S_PIN<327> | -1120.00 | 109.50 |
| 826 | S_PIN<326> | -1136.00 | 213.50 |
| 827 | S_PIN<325> | -1152.00 | 109.50 |
| 828 | S_PIN<324> | -1168.00 | 213.50 |
| 829 | S_PIN<323> | -1184.00 | 109.50 |
| 830 | S_PIN<322> | -1200.00 | 213.50 |
| 831 | S_PIN<321> | -1216.00 | 109.50 |
| 832 | S_PIN<320> | -1232.00 | 213.50 |
| 833 | S_PIN<319> | -1248.00 | 109.50 |
| 834 | S_PIN<318> | -1264.00 | 213.50 |
| 835 | S_PIN<317> | -1280.00 | 109.50 |
| 836 | S_PIN<316> | -1296.00 | 213.50 |
| 837 | S_PIN<315> | -1312.00 | 109.50 |
| 838 | S_PIN<314> | -1328.00 | 213.50 |
| 839 | S_PIN<313> | -1344.00 | 109.50 |
| 840 | S_PIN<312> | -1360.00 | 213.50 |
| 841 | S_PIN<311> | -1376.00 | 109.50 |
| 842 | S_PIN<310> | -1392.00 | 213.50 |
| 843 | S_PIN<309> | -1408.00 | 109.50 |
| 844 | S_PIN<308> | -1424.00 | 213.50 |
| 845 | S_PIN<307> | -1440.00 | 109.50 |
| 846 | S_PIN<306> | -1456.00 | 213.50 |
| 847 | S_PIN<305> | -1472.00 | 109.50 |
| 848 | S_PIN<304> | -1488.00 | 213.50 |
| 849 | S_PIN<303> | -1504.00 | 109.50 |
| 850 | S_PIN<302> | -1520.00 | 213.50 |

| Pad No. | Pad Name | X | Y |
|---------|------------|----------|--------|
| 851 | S_PIN<301> | -1536.00 | 109.50 |
| 852 | S_PIN<300> | -1552.00 | 213.50 |
| 853 | S_PIN<299> | -1568.00 | 109.50 |
| 854 | S_PIN<298> | -1584.00 | 213.50 |
| 855 | S_PIN<297> | -1600.00 | 109.50 |
| 856 | S_PIN<296> | -1616.00 | 213.50 |
| 857 | S_PIN<295> | -1632.00 | 109.50 |
| 858 | S_PIN<294> | -1648.00 | 213.50 |
| 859 | S_PIN<293> | -1664.00 | 109.50 |
| 860 | S_PIN<292> | -1680.00 | 213.50 |
| 861 | S_PIN<291> | -1696.00 | 109.50 |
| 862 | S_PIN<290> | -1712.00 | 213.50 |
| 863 | S_PIN<289> | -1728.00 | 109.50 |
| 864 | S_PIN<288> | -1744.00 | 213.50 |
| 865 | S_PIN<287> | -1760.00 | 109.50 |
| 866 | S_PIN<286> | -1776.00 | 213.50 |
| 867 | S_PIN<285> | -1792.00 | 109.50 |
| 868 | S_PIN<284> | -1808.00 | 213.50 |
| 869 | S_PIN<283> | -1824.00 | 109.50 |
| 870 | S_PIN<282> | -1840.00 | 213.50 |
| 871 | S_PIN<281> | -1856.00 | 109.50 |
| 872 | S_PIN<280> | -1872.00 | 213.50 |
| 873 | S_PIN<279> | -1888.00 | 109.50 |
| 874 | S_PIN<278> | -1904.00 | 213.50 |
| 875 | S_PIN<277> | -1920.00 | 109.50 |
| 876 | S_PIN<276> | -1936.00 | 213.50 |
| 877 | S_PIN<275> | -1952.00 | 109.50 |
| 878 | S_PIN<274> | -1968.00 | 213.50 |
| 879 | S_PIN<273> | -1984.00 | 109.50 |
| 880 | S_PIN<272> | -2000.00 | 213.50 |
| 881 | S_PIN<271> | -2016.00 | 109.50 |
| 882 | S_PIN<270> | -2032.00 | 213.50 |
| 883 | S_PIN<269> | -2048.00 | 109.50 |
| 884 | S_PIN<268> | -2064.00 | 213.50 |
| 885 | S_PIN<267> | -2080.00 | 109.50 |
| 886 | S_PIN<266> | -2096.00 | 213.50 |
| 887 | S_PIN<265> | -2112.00 | 109.50 |
| 888 | S_PIN<264> | -2128.00 | 213.50 |
| 889 | S_PIN<263> | -2144.00 | 109.50 |
| 890 | S_PIN<262> | -2160.00 | 213.50 |
| 891 | S_PIN<261> | -2176.00 | 109.50 |
| 892 | S_PIN<260> | -2192.00 | 213.50 |
| 893 | S_PIN<259> | -2208.00 | 109.50 |
| 894 | S_PIN<258> | -2224.00 | 213.50 |
| 895 | S_PIN<257> | -2240.00 | 109.50 |
| 896 | S_PIN<256> | -2256.00 | 213.50 |
| 897 | S_PIN<255> | -2272.00 | 109.50 |
| 898 | S_PIN<254> | -2288.00 | 213.50 |
| 899 | S_PIN<253> | -2304.00 | 109.50 |
| 900 | S_PIN<252> | -2320.00 | 213.50 |

R61505W PAD Coordinates (unit: um) (No.10)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|------------|----------|--------|
| 901 | S_PIN<251> | -2336.00 | 109.50 |
| 902 | S_PIN<250> | -2352.00 | 213.50 |
| 903 | S_PIN<249> | -2368.00 | 109.50 |
| 904 | S_PIN<248> | -2384.00 | 213.50 |
| 905 | S_PIN<247> | -2400.00 | 109.50 |
| 906 | S_PIN<246> | -2416.00 | 213.50 |
| 907 | S_PIN<245> | -2432.00 | 109.50 |
| 908 | S_PIN<244> | -2448.00 | 213.50 |
| 909 | S_PIN<243> | -2464.00 | 109.50 |
| 910 | S_PIN<242> | -2480.00 | 213.50 |
| 911 | S_PIN<241> | -2496.00 | 109.50 |
| 912 | S_PIN<240> | -2512.00 | 213.50 |
| 913 | S_PIN<239> | -2528.00 | 109.50 |
| 914 | S_PIN<238> | -2544.00 | 213.50 |
| 915 | S_PIN<237> | -2560.00 | 109.50 |
| 916 | S_PIN<236> | -2576.00 | 213.50 |
| 917 | S_PIN<235> | -2592.00 | 109.50 |
| 918 | S_PIN<234> | -2608.00 | 213.50 |
| 919 | S_PIN<233> | -2624.00 | 109.50 |
| 920 | S_PIN<232> | -2640.00 | 213.50 |
| 921 | S_PIN<231> | -2656.00 | 109.50 |
| 922 | S_PIN<230> | -2672.00 | 213.50 |
| 923 | S_PIN<229> | -2688.00 | 109.50 |
| 924 | S_PIN<228> | -2704.00 | 213.50 |
| 925 | S_PIN<227> | -2720.00 | 109.50 |
| 926 | S_PIN<226> | -2736.00 | 213.50 |
| 927 | S_PIN<225> | -2752.00 | 109.50 |
| 928 | S_PIN<224> | -2768.00 | 213.50 |
| 929 | S_PIN<223> | -2784.00 | 109.50 |
| 930 | S_PIN<222> | -2800.00 | 213.50 |
| 931 | S_PIN<221> | -2816.00 | 109.50 |
| 932 | S_PIN<220> | -2832.00 | 213.50 |
| 933 | S_PIN<219> | -2848.00 | 109.50 |
| 934 | S_PIN<218> | -2864.00 | 213.50 |
| 935 | S_PIN<217> | -2880.00 | 109.50 |
| 936 | S_PIN<216> | -2896.00 | 213.50 |
| 937 | S_PIN<215> | -2912.00 | 109.50 |
| 938 | S_PIN<214> | -2928.00 | 213.50 |
| 939 | S_PIN<213> | -2944.00 | 109.50 |
| 940 | S_PIN<212> | -2960.00 | 213.50 |
| 941 | S_PIN<211> | -2976.00 | 109.50 |
| 942 | S_PIN<210> | -2992.00 | 213.50 |
| 943 | S_PIN<209> | -3008.00 | 109.50 |
| 944 | S_PIN<208> | -3024.00 | 213.50 |
| 945 | S_PIN<207> | -3040.00 | 109.50 |
| 946 | S_PIN<206> | -3056.00 | 213.50 |
| 947 | S_PIN<205> | -3072.00 | 109.50 |
| 948 | S_PIN<204> | -3088.00 | 213.50 |
| 949 | S_PIN<203> | -3104.00 | 109.50 |
| 950 | S_PIN<202> | -3120.00 | 213.50 |

| Pad No. | Pad Name | X | Y |
|---------|------------|----------|--------|
| 951 | S_PIN<201> | -3136.00 | 109.50 |
| 952 | S_PIN<200> | -3152.00 | 213.50 |
| 953 | S_PIN<199> | -3168.00 | 109.50 |
| 954 | S_PIN<198> | -3184.00 | 213.50 |
| 955 | S_PIN<197> | -3200.00 | 109.50 |
| 956 | S_PIN<196> | -3216.00 | 213.50 |
| 957 | S_PIN<195> | -3232.00 | 109.50 |
| 958 | S_PIN<194> | -3248.00 | 213.50 |
| 959 | S_PIN<193> | -3264.00 | 109.50 |
| 960 | S_PIN<192> | -3280.00 | 213.50 |
| 961 | S_PIN<191> | -3296.00 | 109.50 |
| 962 | S_PIN<190> | -3312.00 | 213.50 |
| 963 | S_PIN<189> | -3328.00 | 109.50 |
| 964 | S_PIN<188> | -3344.00 | 213.50 |
| 965 | S_PIN<187> | -3360.00 | 109.50 |
| 966 | S_PIN<186> | -3376.00 | 213.50 |
| 967 | S_PIN<185> | -3392.00 | 109.50 |
| 968 | S_PIN<184> | -3408.00 | 213.50 |
| 969 | S_PIN<183> | -3424.00 | 109.50 |
| 970 | S_PIN<182> | -3440.00 | 213.50 |
| 971 | S_PIN<181> | -3456.00 | 109.50 |
| 972 | S_PIN<180> | -3472.00 | 213.50 |
| 973 | S_PIN<179> | -3488.00 | 109.50 |
| 974 | S_PIN<178> | -3504.00 | 213.50 |
| 975 | S_PIN<177> | -3520.00 | 109.50 |
| 976 | S_PIN<176> | -3536.00 | 213.50 |
| 977 | S_PIN<175> | -3552.00 | 109.50 |
| 978 | S_PIN<174> | -3568.00 | 213.50 |
| 979 | S_PIN<173> | -3584.00 | 109.50 |
| 980 | S_PIN<172> | -3600.00 | 213.50 |
| 981 | S_PIN<171> | -3616.00 | 109.50 |
| 982 | S_PIN<170> | -3632.00 | 213.50 |
| 983 | S_PIN<169> | -3648.00 | 109.50 |
| 984 | S_PIN<168> | -3664.00 | 213.50 |
| 985 | S_PIN<167> | -3680.00 | 109.50 |
| 986 | S_PIN<166> | -3696.00 | 213.50 |
| 987 | S_PIN<165> | -3712.00 | 109.50 |
| 988 | S_PIN<164> | -3728.00 | 213.50 |
| 989 | S_PIN<163> | -3744.00 | 109.50 |
| 990 | S_PIN<162> | -3760.00 | 213.50 |
| 991 | S_PIN<161> | -3776.00 | 109.50 |
| 992 | S_PIN<160> | -3792.00 | 213.50 |
| 993 | S_PIN<159> | -3808.00 | 109.50 |
| 994 | S_PIN<158> | -3824.00 | 213.50 |
| 995 | S_PIN<157> | -3840.00 | 109.50 |
| 996 | S_PIN<156> | -3856.00 | 213.50 |
| 997 | S_PIN<155> | -3872.00 | 109.50 |
| 998 | S_PIN<154> | -3888.00 | 213.50 |
| 999 | S_PIN<153> | -3904.00 | 109.50 |
| 1000 | S_PIN<152> | -3920.00 | 213.50 |

R61505W PAD Coordinates (unit: um) (No.11)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|------------|----------|--------|
| 1001 | S_PIN<151> | -3936.00 | 109.50 |
| 1002 | S_PIN<150> | -3952.00 | 213.50 |
| 1003 | S_PIN<149> | -3968.00 | 109.50 |
| 1004 | S_PIN<148> | -3984.00 | 213.50 |
| 1005 | S_PIN<147> | -4000.00 | 109.50 |
| 1006 | S_PIN<146> | -4016.00 | 213.50 |
| 1007 | S_PIN<145> | -4032.00 | 109.50 |
| 1008 | S_PIN<144> | -4048.00 | 213.50 |
| 1009 | S_PIN<143> | -4064.00 | 109.50 |
| 1010 | S_PIN<142> | -4080.00 | 213.50 |
| 1011 | S_PIN<141> | -4096.00 | 109.50 |
| 1012 | S_PIN<140> | -4112.00 | 213.50 |
| 1013 | S_PIN<139> | -4128.00 | 109.50 |
| 1014 | S_PIN<138> | -4144.00 | 213.50 |
| 1015 | S_PIN<137> | -4160.00 | 109.50 |
| 1016 | S_PIN<136> | -4176.00 | 213.50 |
| 1017 | S_PIN<135> | -4192.00 | 109.50 |
| 1018 | S_PIN<134> | -4208.00 | 213.50 |
| 1019 | S_PIN<133> | -4224.00 | 109.50 |
| 1020 | S_PIN<132> | -4240.00 | 213.50 |
| 1021 | S_PIN<131> | -4256.00 | 109.50 |
| 1022 | S_PIN<130> | -4272.00 | 213.50 |
| 1023 | S_PIN<129> | -4288.00 | 109.50 |
| 1024 | S_PIN<128> | -4304.00 | 213.50 |
| 1025 | S_PIN<127> | -4320.00 | 109.50 |
| 1026 | S_PIN<126> | -4336.00 | 213.50 |
| 1027 | S_PIN<125> | -4352.00 | 109.50 |
| 1028 | S_PIN<124> | -4368.00 | 213.50 |
| 1029 | S_PIN<123> | -4384.00 | 109.50 |
| 1030 | S_PIN<122> | -4400.00 | 213.50 |
| 1031 | S_PIN<121> | -4416.00 | 109.50 |
| 1032 | S_PIN<120> | -4432.00 | 213.50 |
| 1033 | S_PIN<119> | -4448.00 | 109.50 |
| 1034 | S_PIN<118> | -4464.00 | 213.50 |
| 1035 | S_PIN<117> | -4480.00 | 109.50 |
| 1036 | S_PIN<116> | -4496.00 | 213.50 |
| 1037 | S_PIN<115> | -4512.00 | 109.50 |
| 1038 | S_PIN<114> | -4528.00 | 213.50 |
| 1039 | S_PIN<113> | -4544.00 | 109.50 |
| 1040 | S_PIN<112> | -4560.00 | 213.50 |
| 1041 | S_PIN<111> | -4576.00 | 109.50 |
| 1042 | S_PIN<110> | -4592.00 | 213.50 |
| 1043 | S_PIN<109> | -4608.00 | 109.50 |
| 1044 | S_PIN<108> | -4624.00 | 213.50 |
| 1045 | S_PIN<107> | -4640.00 | 109.50 |
| 1046 | S_PIN<106> | -4656.00 | 213.50 |
| 1047 | S_PIN<105> | -4672.00 | 109.50 |
| 1048 | S_PIN<104> | -4688.00 | 213.50 |
| 1049 | S_PIN<103> | -4704.00 | 109.50 |
| 1050 | S_PIN<102> | -4720.00 | 213.50 |

| Pad No. | Pad Name | X | Y |
|---------|------------|----------|--------|
| 1051 | S_PIN<101> | -4736.00 | 109.50 |
| 1052 | S_PIN<100> | -4752.00 | 213.50 |
| 1053 | S_PIN<99> | -4768.00 | 109.50 |
| 1054 | S_PIN<98> | -4784.00 | 213.50 |
| 1055 | S_PIN<97> | -4800.00 | 109.50 |
| 1056 | S_PIN<96> | -4816.00 | 213.50 |
| 1057 | S_PIN<95> | -4832.00 | 109.50 |
| 1058 | S_PIN<94> | -4848.00 | 213.50 |
| 1059 | S_PIN<93> | -4864.00 | 109.50 |
| 1060 | S_PIN<92> | -4880.00 | 213.50 |
| 1061 | S_PIN<91> | -4896.00 | 109.50 |
| 1062 | S_PIN<90> | -4912.00 | 213.50 |
| 1063 | S_PIN<89> | -4928.00 | 109.50 |
| 1064 | S_PIN<88> | -4944.00 | 213.50 |
| 1065 | S_PIN<87> | -4960.00 | 109.50 |
| 1066 | S_PIN<86> | -4976.00 | 213.50 |
| 1067 | S_PIN<85> | -4992.00 | 109.50 |
| 1068 | S_PIN<84> | -5008.00 | 213.50 |
| 1069 | S_PIN<83> | -5024.00 | 109.50 |
| 1070 | S_PIN<82> | -5040.00 | 213.50 |
| 1071 | S_PIN<81> | -5056.00 | 109.50 |
| 1072 | S_PIN<80> | -5072.00 | 213.50 |
| 1073 | S_PIN<79> | -5088.00 | 109.50 |
| 1074 | S_PIN<78> | -5104.00 | 213.50 |
| 1075 | S_PIN<77> | -5120.00 | 109.50 |
| 1076 | S_PIN<76> | -5136.00 | 213.50 |
| 1077 | S_PIN<75> | -5152.00 | 109.50 |
| 1078 | S_PIN<74> | -5168.00 | 213.50 |
| 1079 | S_PIN<73> | -5184.00 | 109.50 |
| 1080 | S_PIN<72> | -5200.00 | 213.50 |
| 1081 | S_PIN<71> | -5216.00 | 109.50 |
| 1082 | S_PIN<70> | -5232.00 | 213.50 |
| 1083 | S_PIN<69> | -5248.00 | 109.50 |
| 1084 | S_PIN<68> | -5264.00 | 213.50 |
| 1085 | S_PIN<67> | -5280.00 | 109.50 |
| 1086 | S_PIN<66> | -5296.00 | 213.50 |
| 1087 | S_PIN<65> | -5312.00 | 109.50 |
| 1088 | S_PIN<64> | -5328.00 | 213.50 |
| 1089 | S_PIN<63> | -5344.00 | 109.50 |
| 1090 | S_PIN<62> | -5360.00 | 213.50 |
| 1091 | S_PIN<61> | -5376.00 | 109.50 |
| 1092 | S_PIN<60> | -5392.00 | 213.50 |
| 1093 | S_PIN<59> | -5408.00 | 109.50 |
| 1094 | S_PIN<58> | -5424.00 | 213.50 |
| 1095 | S_PIN<57> | -5440.00 | 109.50 |
| 1096 | S_PIN<56> | -5456.00 | 213.50 |
| 1097 | S_PIN<55> | -5472.00 | 109.50 |
| 1098 | S_PIN<54> | -5488.00 | 213.50 |
| 1099 | S_PIN<53> | -5504.00 | 109.50 |
| 1100 | S_PIN<52> | -5520.00 | 213.50 |

R61505W PAD Coordinates (unit: um) (No.12)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|-----------|----------|--------|
| 1101 | S_PIN<51> | -5536.00 | 109.50 |
| 1102 | S_PIN<50> | -5552.00 | 213.50 |
| 1103 | S_PIN<49> | -5568.00 | 109.50 |
| 1104 | S_PIN<48> | -5584.00 | 213.50 |
| 1105 | S_PIN<47> | -5600.00 | 109.50 |
| 1106 | S_PIN<46> | -5616.00 | 213.50 |
| 1107 | S_PIN<45> | -5632.00 | 109.50 |
| 1108 | S_PIN<44> | -5648.00 | 213.50 |
| 1109 | S_PIN<43> | -5664.00 | 109.50 |
| 1110 | S_PIN<42> | -5680.00 | 213.50 |
| 1111 | S_PIN<41> | -5696.00 | 109.50 |
| 1112 | S_PIN<40> | -5712.00 | 213.50 |
| 1113 | S_PIN<39> | -5728.00 | 109.50 |
| 1114 | S_PIN<38> | -5744.00 | 213.50 |
| 1115 | S_PIN<37> | -5760.00 | 109.50 |
| 1116 | S_PIN<36> | -5776.00 | 213.50 |
| 1117 | S_PIN<35> | -5792.00 | 109.50 |
| 1118 | S_PIN<34> | -5808.00 | 213.50 |
| 1119 | S_PIN<33> | -5824.00 | 109.50 |
| 1120 | S_PIN<32> | -5840.00 | 213.50 |
| 1121 | S_PIN<31> | -5856.00 | 109.50 |
| 1122 | S_PIN<30> | -5872.00 | 213.50 |
| 1123 | S_PIN<29> | -5888.00 | 109.50 |
| 1124 | S_PIN<28> | -5904.00 | 213.50 |
| 1125 | S_PIN<27> | -5920.00 | 109.50 |
| 1126 | S_PIN<26> | -5936.00 | 213.50 |
| 1127 | S_PIN<25> | -5952.00 | 109.50 |
| 1128 | S_PIN<24> | -5968.00 | 213.50 |
| 1129 | S_PIN<23> | -5984.00 | 109.50 |
| 1130 | S_PIN<22> | -6000.00 | 213.50 |
| 1131 | S_PIN<21> | -6016.00 | 109.50 |
| 1132 | S_PIN<20> | -6032.00 | 213.50 |
| 1133 | S_PIN<19> | -6048.00 | 109.50 |
| 1134 | S_PIN<18> | -6064.00 | 213.50 |
| 1135 | S_PIN<17> | -6080.00 | 109.50 |
| 1136 | S_PIN<16> | -6096.00 | 213.50 |
| 1137 | S_PIN<15> | -6112.00 | 109.50 |
| 1138 | S_PIN<14> | -6128.00 | 213.50 |
| 1139 | S_PIN<13> | -6144.00 | 109.50 |
| 1140 | S_PIN<12> | -6160.00 | 213.50 |
| 1141 | S_PIN<11> | -6176.00 | 109.50 |
| 1142 | S_PIN<10> | -6192.00 | 213.50 |
| 1143 | S_PIN<9> | -6208.00 | 109.50 |
| 1144 | S_PIN<8> | -6224.00 | 213.50 |
| 1145 | S_PIN<7> | -6240.00 | 109.50 |
| 1146 | S_PIN<6> | -6256.00 | 213.50 |
| 1147 | S_PIN<5> | -6272.00 | 109.50 |
| 1148 | S_PIN<4> | -6288.00 | 213.50 |
| 1149 | S_PIN<3> | -6304.00 | 109.50 |
| 1150 | S_PIN<2> | -6320.00 | 213.50 |

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|--------|
| 1151 | S_PIN<1> | -6336.00 | 109.50 |
| 1152 | TESTO10 | -6352.00 | 213.50 |
| 1153 | TESTO11 | -6368.00 | 109.50 |
| 1154 | TESTO12 | -6560.00 | 213.50 |
| 1155 | VGLDMY3 | -6576.00 | 109.50 |
| 1156 | G<320> | -6592.00 | 213.50 |
| 1157 | G<318> | -6608.00 | 109.50 |
| 1158 | G<316> | -6624.00 | 213.50 |
| 1159 | G<314> | -6640.00 | 109.50 |
| 1160 | G<312> | -6656.00 | 213.50 |
| 1161 | G<310> | -6672.00 | 109.50 |
| 1162 | G<308> | -6688.00 | 213.50 |
| 1163 | G<306> | -6704.00 | 109.50 |
| 1164 | G<304> | -6720.00 | 213.50 |
| 1165 | G<302> | -6736.00 | 109.50 |
| 1166 | G<300> | -6752.00 | 213.50 |
| 1167 | G<298> | -6768.00 | 109.50 |
| 1168 | G<296> | -6784.00 | 213.50 |
| 1169 | G<294> | -6800.00 | 109.50 |
| 1170 | G<292> | -6816.00 | 213.50 |
| 1171 | G<290> | -6832.00 | 109.50 |
| 1172 | G<288> | -6848.00 | 213.50 |
| 1173 | G<286> | -6864.00 | 109.50 |
| 1174 | G<284> | -6880.00 | 213.50 |
| 1175 | G<282> | -6896.00 | 109.50 |
| 1176 | G<280> | -6912.00 | 213.50 |
| 1177 | G<278> | -6928.00 | 109.50 |
| 1178 | G<276> | -6944.00 | 213.50 |
| 1179 | G<274> | -6960.00 | 109.50 |
| 1180 | G<272> | -6976.00 | 213.50 |
| 1181 | G<270> | -6992.00 | 109.50 |
| 1182 | G<268> | -7008.00 | 213.50 |
| 1183 | G<266> | -7024.00 | 109.50 |
| 1184 | G<264> | -7040.00 | 213.50 |
| 1185 | G<262> | -7056.00 | 109.50 |
| 1186 | G<260> | -7072.00 | 213.50 |
| 1187 | G<258> | -7088.00 | 109.50 |
| 1188 | G<256> | -7104.00 | 213.50 |
| 1189 | G<254> | -7120.00 | 109.50 |
| 1190 | G<252> | -7136.00 | 213.50 |
| 1191 | G<250> | -7152.00 | 109.50 |
| 1192 | G<248> | -7168.00 | 213.50 |
| 1193 | G<246> | -7184.00 | 109.50 |
| 1194 | G<244> | -7200.00 | 213.50 |
| 1195 | G<242> | -7216.00 | 109.50 |
| 1196 | G<240> | -7232.00 | 213.50 |
| 1197 | G<238> | -7248.00 | 109.50 |
| 1198 | G<236> | -7264.00 | 213.50 |
| 1199 | G<234> | -7280.00 | 109.50 |
| 1200 | G<232> | -7296.00 | 213.50 |

R61505W PAD Coordinates (unit: um) (No.13)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|--------|
| 1201 | G<230> | -7312.00 | 109.50 |
| 1202 | G<228> | -7328.00 | 213.50 |
| 1203 | G<226> | -7344.00 | 109.50 |
| 1204 | G<224> | -7360.00 | 213.50 |
| 1205 | G<222> | -7376.00 | 109.50 |
| 1206 | G<220> | -7392.00 | 213.50 |
| 1207 | G<218> | -7408.00 | 109.50 |
| 1208 | G<216> | -7424.00 | 213.50 |
| 1209 | G<214> | -7440.00 | 109.50 |
| 1210 | G<212> | -7456.00 | 213.50 |
| 1211 | G<210> | -7472.00 | 109.50 |
| 1212 | G<208> | -7488.00 | 213.50 |
| 1213 | G<206> | -7504.00 | 109.50 |
| 1214 | G<204> | -7520.00 | 213.50 |
| 1215 | G<202> | -7536.00 | 109.50 |
| 1216 | G<200> | -7552.00 | 213.50 |
| 1217 | G<198> | -7568.00 | 109.50 |
| 1218 | G<196> | -7584.00 | 213.50 |
| 1219 | G<194> | -7600.00 | 109.50 |
| 1220 | G<192> | -7616.00 | 213.50 |
| 1221 | G<190> | -7632.00 | 109.50 |
| 1222 | G<188> | -7648.00 | 213.50 |
| 1223 | G<186> | -7664.00 | 109.50 |
| 1224 | G<184> | -7680.00 | 213.50 |
| 1225 | G<182> | -7696.00 | 109.50 |
| 1226 | G<180> | -7712.00 | 213.50 |
| 1227 | G<178> | -7728.00 | 109.50 |
| 1228 | G<176> | -7744.00 | 213.50 |
| 1229 | G<174> | -7760.00 | 109.50 |
| 1230 | G<172> | -7776.00 | 213.50 |
| 1231 | G<170> | -7792.00 | 109.50 |
| 1232 | G<168> | -7808.00 | 213.50 |
| 1233 | G<166> | -7824.00 | 109.50 |
| 1234 | G<164> | -7840.00 | 213.50 |
| 1235 | G<162> | -7856.00 | 109.50 |
| 1236 | G<160> | -7872.00 | 213.50 |
| 1237 | G<158> | -7888.00 | 109.50 |
| 1238 | G<156> | -7904.00 | 213.50 |
| 1239 | G<154> | -7920.00 | 109.50 |
| 1240 | G<152> | -7936.00 | 213.50 |
| 1241 | G<150> | -7952.00 | 109.50 |
| 1242 | G<148> | -7968.00 | 213.50 |
| 1243 | G<146> | -7984.00 | 109.50 |
| 1244 | G<144> | -8000.00 | 213.50 |
| 1245 | G<142> | -8016.00 | 109.50 |
| 1246 | G<140> | -8032.00 | 213.50 |
| 1247 | G<138> | -8048.00 | 109.50 |
| 1248 | G<136> | -8064.00 | 213.50 |
| 1249 | G<134> | -8080.00 | 109.50 |
| 1250 | G<132> | -8096.00 | 213.50 |

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|--------|
| 1251 | G<130> | -8112.00 | 109.50 |
| 1252 | G<128> | -8128.00 | 213.50 |
| 1253 | G<126> | -8144.00 | 109.50 |
| 1254 | G<124> | -8160.00 | 213.50 |
| 1255 | G<122> | -8176.00 | 109.50 |
| 1256 | G<120> | -8192.00 | 213.50 |
| 1257 | G<118> | -8208.00 | 109.50 |
| 1258 | G<116> | -8224.00 | 213.50 |
| 1259 | G<114> | -8240.00 | 109.50 |
| 1260 | G<112> | -8256.00 | 213.50 |
| 1261 | G<110> | -8272.00 | 109.50 |
| 1262 | G<108> | -8288.00 | 213.50 |
| 1263 | G<106> | -8304.00 | 109.50 |
| 1264 | G<104> | -8320.00 | 213.50 |
| 1265 | G<102> | -8336.00 | 109.50 |
| 1266 | G<100> | -8352.00 | 213.50 |
| 1267 | G<98> | -8368.00 | 109.50 |
| 1268 | G<96> | -8384.00 | 213.50 |
| 1269 | G<94> | -8400.00 | 109.50 |
| 1270 | G<92> | -8416.00 | 213.50 |
| 1271 | G<90> | -8432.00 | 109.50 |
| 1272 | G<88> | -8448.00 | 213.50 |
| 1273 | G<86> | -8464.00 | 109.50 |
| 1274 | G<84> | -8480.00 | 213.50 |
| 1275 | G<82> | -8496.00 | 109.50 |
| 1276 | G<80> | -8512.00 | 213.50 |
| 1277 | G<78> | -8528.00 | 109.50 |
| 1278 | G<76> | -8544.00 | 213.50 |
| 1279 | G<74> | -8560.00 | 109.50 |
| 1280 | G<72> | -8576.00 | 213.50 |
| 1281 | G<70> | -8592.00 | 109.50 |
| 1282 | G<68> | -8608.00 | 213.50 |
| 1283 | G<66> | -8624.00 | 109.50 |
| 1284 | G<64> | -8640.00 | 213.50 |
| 1285 | G<62> | -8656.00 | 109.50 |
| 1286 | G<60> | -8672.00 | 213.50 |
| 1287 | G<58> | -8688.00 | 109.50 |
| 1288 | G<56> | -8704.00 | 213.50 |
| 1289 | G<54> | -8720.00 | 109.50 |
| 1290 | G<52> | -8736.00 | 213.50 |
| 1291 | G<50> | -8752.00 | 109.50 |
| 1292 | G<48> | -8768.00 | 213.50 |
| 1293 | G<46> | -8784.00 | 109.50 |
| 1294 | G<44> | -8800.00 | 213.50 |
| 1295 | G<42> | -8816.00 | 109.50 |
| 1296 | G<40> | -8832.00 | 213.50 |
| 1297 | G<38> | -8848.00 | 109.50 |
| 1298 | G<36> | -8864.00 | 213.50 |
| 1299 | G<34> | -8880.00 | 109.50 |
| 1300 | G<32> | -8896.00 | 213.50 |

R61505W PAD Coordinates (unit: um) (No.14)

2009.2.23 Rev.1.00

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|--------|
| 1301 | G<30> | -8912.00 | 109.50 |
| 1302 | G<28> | -8928.00 | 213.50 |
| 1303 | G<26> | -8944.00 | 109.50 |
| 1304 | G<24> | -8960.00 | 213.50 |
| 1305 | G<22> | -8976.00 | 109.50 |
| 1306 | G<20> | -8992.00 | 213.50 |
| 1307 | G<18> | -9008.00 | 109.50 |
| 1308 | G<16> | -9024.00 | 213.50 |
| 1309 | G<14> | -9040.00 | 109.50 |
| 1310 | G<12> | -9056.00 | 213.50 |
| 1311 | G<10> | -9072.00 | 109.50 |
| 1312 | G<8> | -9088.00 | 213.50 |
| 1313 | G<6> | -9104.00 | 109.50 |
| 1314 | G<4> | -9120.00 | 213.50 |
| 1315 | G<2> | -9136.00 | 109.50 |
| 1316 | VGLDMY4 | -9152.00 | 213.50 |
| 1317 | DUMMYR5 | -9168.00 | 109.50 |
| 1318 | DUMMYR6 | -9184.00 | 213.50 |
| 1319 | TESTO13 | -9200.00 | 109.50 |
| 1320 | TESTO14 | -9216.00 | 213.50 |

Bump Arrangement

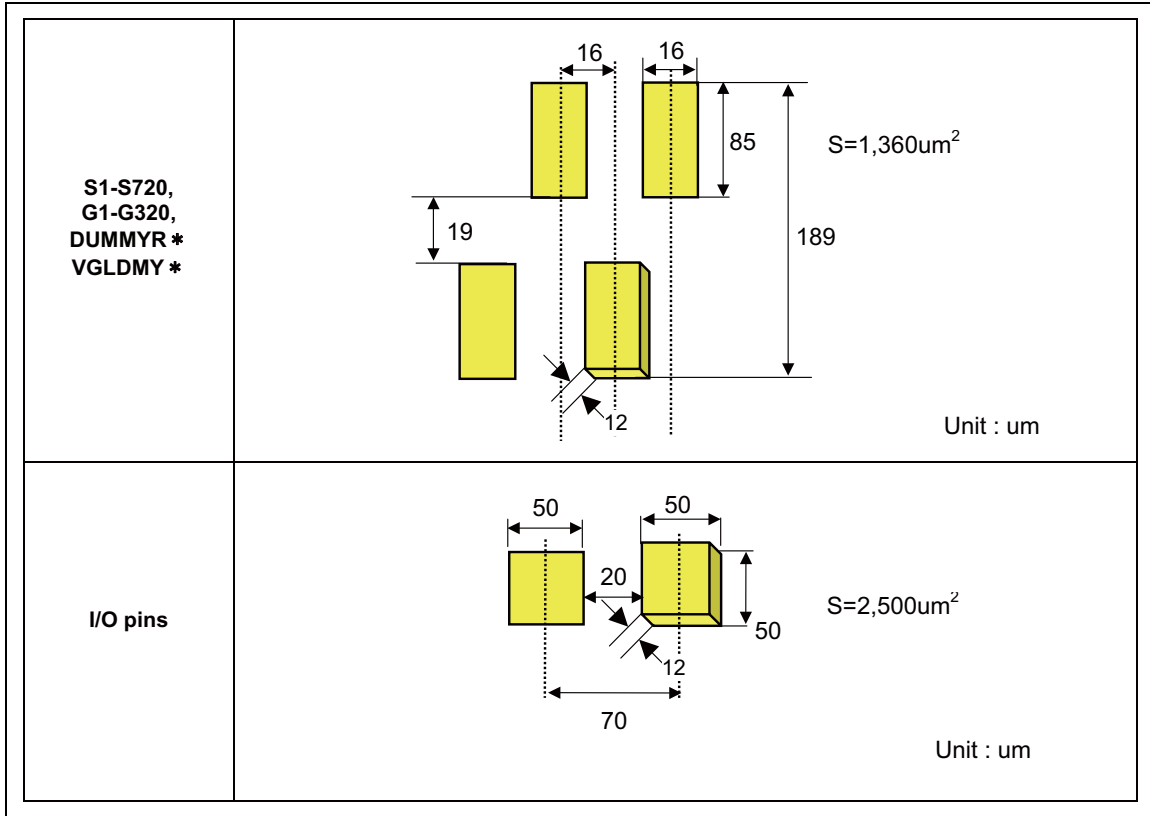
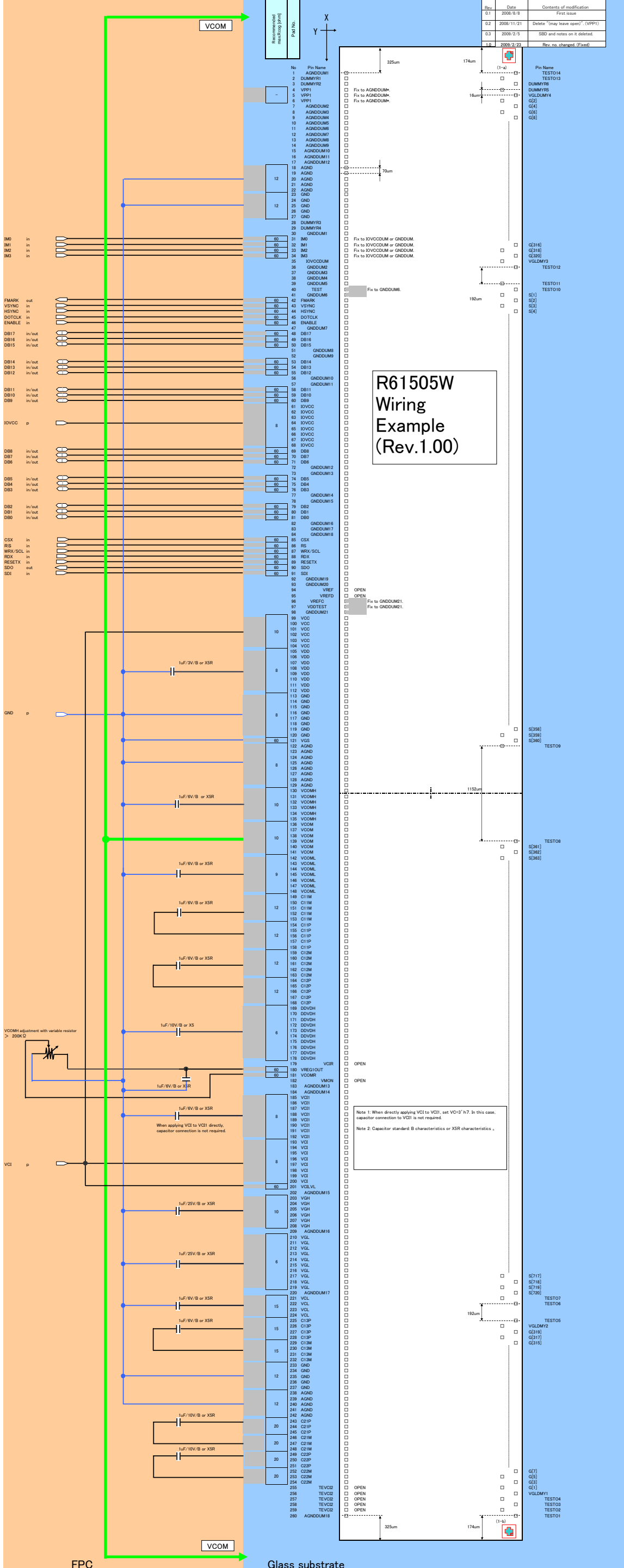


Figure 3

R61505W Wiring Example & Recommended Wiring Resistance



Frame Memory Address Map

Table 13 Frame Memory Address and Display Position on the Panel (SS = 0, BGR = 0)

| S/G pin | | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | | S709 | S710 | S711 | S712 | S713 | S714 | S715 | S716 | S717 | S718 | S719 | S720 |
|---------|------|----------|----|----|----------|----|----|----------|----|----|----------|-----|-----|-------|----------|------|------|----------|------|------|----------|------|------|----------|------|------|
| GS=0 | GS=1 | WD[17:0] | | | WD[17:0] | | | WD[17:0] | | | WD[17:0] | | | | WD[17:0] | | | WD[17:0] | | | WD[17:0] | | | WD[17:0] | | |
| G1 | G320 | h00000 | | | h00001 | | | h00002 | | | h00003 | | | | h000EC | | | h000ED | | | h000EE | | | h000EF | | |
| G2 | G319 | h00100 | | | h00101 | | | h00102 | | | h00103 | | | | h001EC | | | h001ED | | | h001EE | | | h001EF | | |
| G3 | G318 | h00200 | | | h00201 | | | h00202 | | | h00203 | | | | h002EC | | | h002ED | | | h002EE | | | h002EF | | |
| G4 | G317 | h00300 | | | h00301 | | | h00302 | | | h00303 | | | | h003EC | | | h003ED | | | h003EE | | | h003EF | | |
| G5 | G316 | h00400 | | | h00401 | | | h00402 | | | h00403 | | | | h004EC | | | h004ED | | | h004EE | | | h004EF | | |
| G6 | G315 | h00500 | | | h00501 | | | h00502 | | | h00503 | | | | h005EC | | | h005ED | | | h005EE | | | h005EF | | |
| G7 | G314 | h00600 | | | h00601 | | | h00602 | | | h00603 | | | | h006EC | | | h006ED | | | h006EE | | | h006EF | | |
| G8 | G313 | h00700 | | | h00701 | | | h00702 | | | h00703 | | | | h007EC | | | h007ED | | | h007EE | | | h007EF | | |
| G9 | G312 | h00800 | | | h00801 | | | h00802 | | | h00803 | | | | h008EC | | | h008ED | | | h008EE | | | h008EF | | |
| G10 | G311 | h00900 | | | h00901 | | | h00902 | | | h00903 | | | | h009EC | | | h009ED | | | h009EE | | | h009EF | | |
| G11 | G310 | h00A00 | | | h00A01 | | | h00A02 | | | h00A03 | | | | h00AEC | | | h00AED | | | h00AEE | | | h00AEF | | |
| G12 | G309 | h00B00 | | | h00B01 | | | h00B02 | | | h00B03 | | | | h00BEC | | | h00BED | | | h00BEE | | | h00BEF | | |
| G13 | G308 | h00C00 | | | h00C01 | | | h00C02 | | | h00C03 | | | | h00CEC | | | h00CED | | | h00CEE | | | h00CEF | | |
| G14 | G307 | h00D00 | | | h00D01 | | | h00D02 | | | h00D03 | | | | h00DEC | | | h00DED | | | h00DEE | | | h00DEF | | |
| G15 | G306 | h00E00 | | | h00E01 | | | h00E02 | | | h00E03 | | | | h00EEC | | | h00EED | | | h00EEE | | | h00EEF | | |
| G16 | G305 | h00F00 | | | h00F01 | | | h00F02 | | | h00F03 | | | | h00FEC | | | h00FED | | | h00FEE | | | h00FEF | | |
| G17 | G304 | h01000 | | | h01001 | | | h01002 | | | h01003 | | | | h010EC | | | h010ED | | | h010EE | | | h010EF | | |
| G18 | G303 | h01100 | | | h01101 | | | h01102 | | | h01103 | | | | h011EC | | | h011ED | | | h011EE | | | h011EF | | |
| G19 | G302 | h01200 | | | h01201 | | | h01202 | | | h01203 | | | | h012EC | | | h012ED | | | h012EE | | | h012EF | | |
| G20 | G301 | h01300 | | | h01301 | | | h01302 | | | h01303 | | | | h013EC | | | h013ED | | | h013EE | | | h013EF | | |
| : | : | : | | | : | | | : | | | : | | | : | : | | | : | | | : | | | : | | |
| G305 | G16 | h13000 | | | h13001 | | | h13002 | | | h13003 | | | | h130EC | | | h130ED | | | h130EE | | | h130EF | | |
| G306 | G15 | h13100 | | | h13101 | | | h13102 | | | h13103 | | | | h131EC | | | h131ED | | | h131EE | | | h131EF | | |
| G307 | G14 | h13200 | | | h13201 | | | h13202 | | | h13203 | | | | h132EC | | | h132ED | | | h132EE | | | h132EF | | |
| G308 | G13 | h13300 | | | h13301 | | | h13302 | | | h13303 | | | | h133EC | | | h133ED | | | h133EE | | | h133EF | | |
| G309 | G12 | h13400 | | | h13401 | | | h13402 | | | h13403 | | | | h134EC | | | h134ED | | | h134EE | | | h134EF | | |
| G310 | G11 | h13500 | | | h13501 | | | h13502 | | | h13503 | | | | h135EC | | | h135ED | | | h135EE | | | h135EF | | |
| G311 | G10 | h13600 | | | h13601 | | | h13602 | | | h13603 | | | | h136EC | | | h136ED | | | h136EE | | | h136EF | | |
| G312 | G9 | h13700 | | | h13701 | | | h13702 | | | h13703 | | | | h137EC | | | h137ED | | | h137EE | | | h137EF | | |
| G313 | G8 | h13800 | | | h13801 | | | h13802 | | | h13803 | | | | h138EC | | | h138ED | | | h138EE | | | h138EF | | |
| G314 | G7 | h13900 | | | h13901 | | | h13902 | | | h13903 | | | | h139EC | | | h139ED | | | h139EE | | | h139EF | | |
| G315 | G6 | h13A00 | | | h13A01 | | | h13A02 | | | h13A03 | | | | h13AEC | | | h13AED | | | h13AEE | | | h13AEF | | |
| G316 | G5 | h13B00 | | | h13B01 | | | h13B02 | | | h13B03 | | | | h13BEC | | | h13BED | | | h13BEE | | | h13BEF | | |
| G317 | G4 | h13C00 | | | h13C01 | | | h13C02 | | | h13C03 | | | | h13CEC | | | h13CED | | | h13CEE | | | h13CEF | | |
| G318 | G3 | h13D00 | | | h13D01 | | | h13D02 | | | h13D03 | | | | h13DEC | | | h13DED | | | h13DEE | | | h13DEF | | |
| G319 | G2 | h13E00 | | | h13E01 | | | h13E02 | | | h13E03 | | | | h13EEC | | | h13EED | | | h13EEE | | | h13EEF | | |
| G320 | G1 | h13F00 | | | h13F01 | | | h13F02 | | | h13F03 | | | | h13FEC | | | h13FED | | | h13FEE | | | h13FEF | | |

Table 14 Frame Memory Address and Display Position on the Panel (SS = 1, BGR = 1)

| S/G pin | | S720 | S719 | S718 | S717 | S716 | S715 | S714 | S713 | S712 | S711 | S710 | S709 | | S12 | S11 | S10 | S9 | S8 | S7 | S6 | S5 | S4 | S3 | S2 | S1 | | | |
|---------|------|----------|------|------|----------|------|------|----------|------|------|----------|------|------|-------|----------|-----|-----|----------|----|----|----------|----|----|----------|----|----|----------|--|--|
| GS=0 | GS=1 | WD[17:0] | | | WD[17:0] | | | WD[17:0] | | | WD[17:0] | | | | WD[17:0] | | | WD[17:0] | | | WD[17:0] | | | WD[17:0] | | | WD[17:0] | | |
| G1 | G320 | h00000 | | | h00001 | | | h00002 | | | h00003 | | | | h000EC | | | h000ED | | | h000EE | | | h000EF | | | | | |
| G2 | G319 | h00100 | | | h00101 | | | h00102 | | | h00103 | | | | h001EC | | | h001ED | | | h001EE | | | h001EF | | | | | |
| G3 | G318 | h00200 | | | h00201 | | | h00202 | | | h00203 | | | | h002EC | | | h002ED | | | h002EE | | | h002EF | | | | | |
| G4 | G317 | h00300 | | | h00301 | | | h00302 | | | h00303 | | | | h003EC | | | h003ED | | | h003EE | | | h003EF | | | | | |
| G5 | G316 | h00400 | | | h00401 | | | h00402 | | | h00403 | | | | h004EC | | | h004ED | | | h004EE | | | h004EF | | | | | |
| G6 | G315 | h00500 | | | h00501 | | | h00502 | | | h00503 | | | | h005EC | | | h005ED | | | h005EE | | | h005EF | | | | | |
| G7 | G314 | h00600 | | | h00601 | | | h00602 | | | h00603 | | | | h006EC | | | h006ED | | | h006EE | | | h006EF | | | | | |
| G8 | G313 | h00700 | | | h00701 | | | h00702 | | | h00703 | | | | h007EC | | | h007ED | | | h007EE | | | h007EF | | | | | |
| G9 | G312 | h00800 | | | h00801 | | | h00802 | | | h00803 | | | | h008EC | | | h008ED | | | h008EE | | | h008EF | | | | | |
| G10 | G311 | h00900 | | | h00901 | | | h00902 | | | h00903 | | | | h009EC | | | h009ED | | | h009EE | | | h009EF | | | | | |
| G11 | G310 | h00A00 | | | h00A01 | | | h00A02 | | | h00A03 | | | | h00AEC | | | h00AED | | | h00AEE | | | h00AEF | | | | | |
| G12 | G309 | h00B00 | | | h00B01 | | | h00B02 | | | h00B03 | | | | h00BEC | | | h00BED | | | h00BEE | | | h00BEF | | | | | |
| G13 | G308 | h00C00 | | | h00C01 | | | h00C02 | | | h00C03 | | | | h00CEC | | | h00CED | | | h00CEE | | | h00CEF | | | | | |
| G14 | G307 | h00D00 | | | h00D01 | | | h00D02 | | | h00D03 | | | | h00DEC | | | h00DED | | | h00DEE | | | h00DEF | | | | | |
| G15 | G306 | h00E00 | | | h00E01 | | | h00E02 | | | h00E03 | | | | h00EEC | | | h00EED | | | h00EEE | | | h00EEF | | | | | |
| G16 | G305 | h00F00 | | | h00F01 | | | h00F02 | | | h00F03 | | | | h00FEC | | | h00FED | | | h00FEE | | | h00FEF | | | | | |
| G17 | G304 | h01000 | | | h01001 | | | h01002 | | | h01003 | | | | h010EC | | | h010ED | | | h010EE | | | h010EF | | | | | |
| G18 | G303 | h01100 | | | h01101 | | | h01102 | | | h01103 | | | | h011EC | | | h011ED | | | h011EE | | | h011EF | | | | | |
| G19 | G302 | h01200 | | | h01201 | | | h01202 | | | h01203 | | | | h012EC | | | h012ED | | | h012EE | | | h012EF | | | | | |
| G20 | G301 | h01300 | | | h01301 | | | h01302 | | | h01303 | | | | h013EC | | | h013ED | | | h013EE | | | h013EF | | | | | |
| : | : | : | | | : | | | : | | | : | | | : | : | | | : | | | : | | | : | | | : | | |
| G305 | G16 | h13000 | | | h13001 | | | h13002 | | | h13003 | | | | h130EC | | | h130ED | | | h130EE | | | h130EF | | | | | |
| G306 | G15 | h13100 | | | h13101 | | | h13102 | | | h13103 | | | | h131EC | | | h131ED | | | h131EE | | | h131EF | | | | | |
| G307 | G14 | h13200 | | | h13201 | | | h13202 | | | h13203 | | | | h132EC | | | h132ED | | | h132EE | | | h132EF | | | | | |
| G308 | G13 | h13300 | | | h13301 | | | h13302 | | | h13303 | | | | h133EC | | | h133ED | | | h133EE | | | h133EF | | | | | |
| G309 | G12 | h13400 | | | h13401 | | | h13402 | | | h13403 | | | | h134EC | | | h134ED | | | h134EE | | | h134EF | | | | | |
| G310 | G11 | h13500 | | | h13501 | | | h13502 | | | h13503 | | | | h135EC | | | h135ED | | | h135EE | | | h135EF | | | | | |
| G311 | G10 | h13600 | | | h13601 | | | h13602 | | | h13603 | | | | h136EC | | | h136ED | | | h136EE | | | h136EF | | | | | |
| G312 | G9 | h13700 | | | h13701 | | | h13702 | | | h13703 | | | | h137EC | | | h137ED | | | h137EE | | | h137EF | | | | | |
| G313 | G8 | h13800 | | | h13801 | | | h13802 | | | h13803 | | | | h138EC | | | h138ED | | | h138EE | | | h138EF | | | | | |
| G314 | G7 | h13900 | | | h13901 | | | h13902 | | | h13903 | | | | h139EC | | | h139ED | | | h139EE | | | h139EF | | | | | |
| G315 | G6 | h13A00 | | | h13A01 | | | h13A02 | | | h13A03 | | | | h13AEC | | | h13AED | | | h13AEE | | | h13AEF | | | | | |
| G316 | G5 | h13B00 | | | h13B01 | | | h13B02 | | | h13B03 | | | | h13BEC | | | h13BED | | | h13BEE | | | h13BEF | | | | | |
| G317 | G4 | h13C00 | | | h13C01 | | | h13C02 | | | h13C03 | | | | h13CEC | | | h13CED | | | h13CEE | | | h13CEF | | | | | |
| G318 | G3 | h13D00 | | | h13D01 | | | h13D02 | | | h13D03 | | | | h13DEC | | | h13DED | | | h13DEE | | | h13DEF | | | | | |
| G319 | G2 | h13E00 | | | h13E01 | | | h13E02 | | | h13E03 | | | | h13EEC | | | h13EED | | | h13EEE | | | h13EEF | | | | | |
| G320 | G1 | h13F00 | | | h13F01 | | | h13F02 | | | h13F03 | | | | h13FEC | | | h13FED | | | h13FEE | | | h13FEF | | | | | |

Instruction

Outline

The R61505W adopts 18-bit bus architecture in order to interface to high-performance host processor in high speed. The R61505W starts internal processing after storing 16-/18-bit control information sent from the host processor, in the instruction register (IR) and the data register (DR). Since the internal operation of the R61505W is controlled by the signals sent from the host processor, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB[15:0]) are called instruction. The following are the kinds of instruction of the R61505W.

1. Specify index
2. Display control
3. Power management control
4. Set internal frame memory address
5. Transfer data to and from the internal frame memory
6. γ -correction
7. Window address control
8. Panel Display Control

Normally, the instruction to write data is used the most often. The internal frame memory address is updated automatically as data is written to the internal frame memory, which, in combination with the window address function, contributes to minimizing data transfer and thereby lessens the load on the host processor. The R61505W writes instructions consecutively by executing the instruction within the cycle when it is written (instruction execution time: 0 cycles).

Instruction Data Format

As the following figure shows, the data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface.

The following are detail descriptions of instruction bits (IB[15:0]). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface.

The bits to which no instruction is assigned must be set to either “0” or “1” according to the following register tables. When changing only one instruction bit setting, the setting values in other bits in the register must be written.

Index (IR)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| W | 0 | * | * | * | * | * | * | * | * | ID [7] | ID [6] | ID [5] | ID [4] | ID [3] | ID [2] | ID [1] | ID [0] |

The index register specifies the index R00h to RFFh of the control register or frame memory control to be accessed using a binary number from “0000_0000” to “1111_1111”. The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.

Display Control**Device Code Read (R00h)**

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

The device code “C505”h is read out when reading out this register forcibly.

Driver Output Control (R01h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | 0 | 0 | SM | 0 | SS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SS: Sets the shift direction of output from the source driver.

When SS = “0”, the source driver output shifts from S1 to S720.

When SS = “1”, the source driver output shifts from S720 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = “0” and BGR = “0”, color data is output in the order of R, G and then B.

When SS = “1” and BGR = “1”, color data is output in the order of B, G and then R.

When changing the SS and the BGR bit settings, frame memory data must be rewritten.

SM: Controls the scan mode in combination with GS setting. See “Scan Mode Setting”.

LCD Driving Wave Control (R02h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | BC0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NW0 |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

NW0: When line inversion waveform is selected (BC0=1), NW0 bit sets number of line, N, as alternating cycle of line inversion. Line inversion is operated every N+1 line cycle. NW0 bit can be set to 1 or 2.

Table 15

| NW[0] | Alternating cycle |
|-------|-------------------|
| 0 | Every line |
| 1 | Every 2 lines |

BC0: Selects the liquid crystal drive waveform VCOM. See “Line Inversion AC Drive” for details.

BC0 = 0: frame inversion waveform is selected.

BC0 = 1: line inversion waveform is selected.

In either liquid crystal drive method, the polarity inversion is halted in blank period (back and front porch periods).

Entry Mode (R03h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------------|------|------|------|------|------|-----|-----|-----|-----|------------|------------|-----|-----|-----|-----|
| W | 1 | TRIR EG | DFM | 0 | BGR | 0 | 0 | 0 | 0 | ORG | 0 | I/D [1] | I/D [0] | AM | 0 | 0 | 0 |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

The entry mode register includes instruction bits for setting how to write data from the host processor to the frame memory in the R61505W.

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the R61505W writes data to the internal frame memory.

AM = "0", sets the horizontal direction.

AM = "1", sets the vertical direction.

When making a window address area, the data is written only within the area in the direction determined by I/D[1:0] and AM bits.

I/D[1:0]: Either increments (+1) or decrements (-1) the address counter (AC) automatically as the data is written to the frame memory. The I/D[0] bit sets either increment or decrement in horizontal direction (updates the address AD[7:0]). The I/D[1] bit sets either increment or decrement in vertical direction (updates the address AD[8:16]). The AM bit sets either horizontal or vertical direction in updating frame memory address counter automatically when writing data to the internal frame memory.

ORG: Moves the origin address according to the I/D setting when a window address area is made. This function is enabled when writing data within the window address area using high-speed frame memory write function. Also see Figure 4 and Figure 5.

ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the frame memory address map within the window address area.

ORG = 1: The origin address "h00000" is moved according to the I/D[1:0] setting.

- Notes: 1. When ORG = 1, only the origin address "h00000" can be set.
2. In frame memory read operation, make sure to set ORG = 0.

BGR: Reverses the order from RGB to BGR in writing 18-bit pixel data in the frame memory.

BGR = 0: Write data in the order of RGB to the frame memory.

BGR = 1: Reverse the order from RGB to BGR in writing data to the frame memory.

BGR = 0

| | | | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |

BGR = 1

| | | | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| B5 | B4 | B3 | B2 | B1 | B0 | G5 | G4 | G3 | G2 | G1 | G0 | R5 | R4 | R3 | R2 | R1 | R0 |

DFM: In combination with the TRIREG setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface. Make sure to set DFM = 0 when not transferring data via 16-bit or 8-bit interface.

TRIREG: Selects the format to transfer data bits via 16-bit or 8-bit interface.

In 80-system 8-bit interface operation,

TRIREG = 0: 16-bit frame memory data is transferred in two transfers.

TRIREG = 1: 18-bit frame memory data is transferred in three transfers.

In 80-system 16-bit bus interface operation,

TRIREG = 0: 16-bit frame memory data is transferred in one transfer.

TRIREG = 1: 18-bit frame memory data is transferred in two transfers.

Make sure TRIREG = 0 when not transferring data via 16-bit or 8-bit interface. Also, set TRIREG = 0 during read operation.

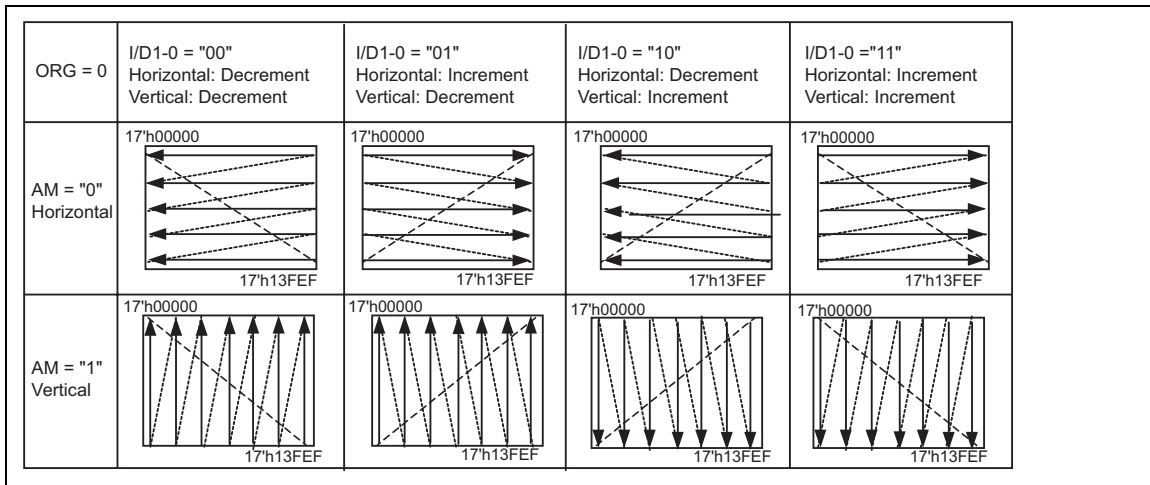


Figure 4 Automatic Address Update (ORG = 0, AM, I/D)

Note: When writing data within the window address area with ORG = 0, any address within the window address area can be designated as the starting point of frame memory write operation.

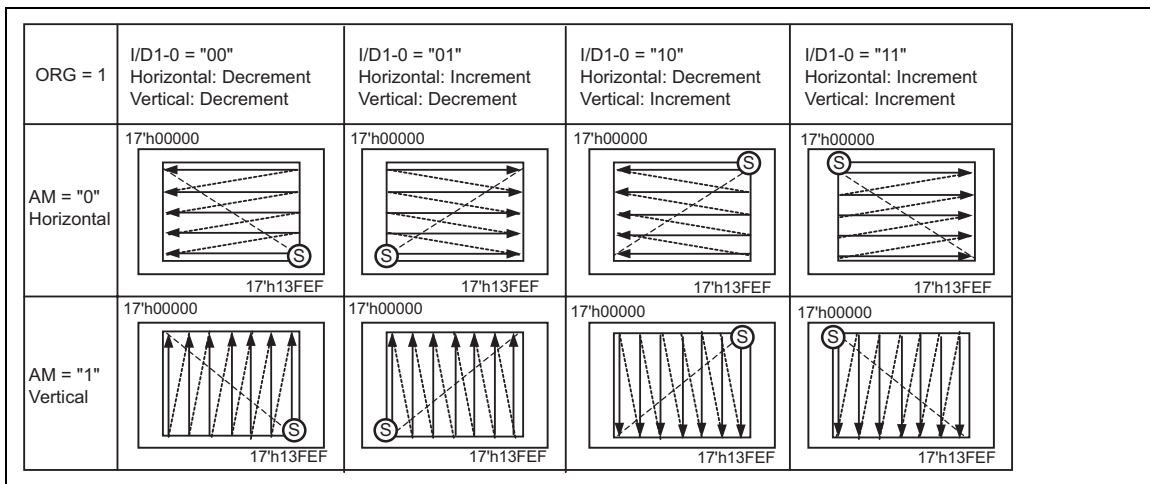


Figure 5 Automatic Address Update (ORG = 1, AM, I/D)

- Notes:
1. When ORG = 1, the starting point of writing data within the window address area can be set at either corner of the window address area ("S" in circle in the above figure).
 2. When ORG = 1, make sure to set the address "h00000" in the frame memory address set registers (R210 and R21h). Setting other addresses is inhibited.

Display Control 1 (R07h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------|-----|-----------|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | PTDE | 0 | 0 | 0 | BASE E | 0 | 0 | 0 | 0 | COL | 0 | 0 | 0 |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

COL: When COL = 1, grayscale amplifiers other than V0 and V63 halt displaying images so that power consumption is reduced. Also, only 8 colors are available. See “8-Color Display Mode” in “Instruction Setting Sequence” for details.

Table 16

| COL | Display color |
|-----|---------------|
| 0 | 262,144 |
| 1 | 8 |

Note: When COL = 1, do not write the data corresponding to the grayscales, for which the operation of amplifier is halted.

BASEE: Base image display enable bit.

BASEE = 0: No base image is displayed. The R61505W drives liquid crystal with non-lit display level or drives only partial image display area.

BASEE = 1: A base image is displayed on the panel.

PTDE: PTDE is the display enable bit of a partial image.

PTDE=0: Partial image is not displayed. Only base image is displayed.

PTDE=1: Partial image is displayed. Write BASEE=0 to turn off a base image.

Table 17

| BASEE | PTDE | VLE | COL | State |
|-------|------|-----|-----|--|
| 0 | 0 | * | * | Halt display operation |
| 1 | 0 | 0 | 0 | 262,144-color display operation |
| 1 | 0 | 0 | 1 | 8-color display operation |
| 1 | 0 | 1 | 0 | 262,144-color display operation with scroll function enabled |
| 0 | 1 | * | 0 | 262,144-color partial display operation |
| 0 | 1 | * | 1 | 8-color partial display operation |

Display Control 2 (R08h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W | 1 | FP [7] | FP [6] | FP [5] | FP [4] | FP [3] | FP [2] | FP [1] | FP [0] | BP [7] | BP [6] | BP [5] | BP [4] | BP [3] | BP [2] | BP [1] | BP [0] |
| Default value | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

FP [7:0]: Sets the number of lines for a front porch period (a blank period following the end of display).

BP [7:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

Table 18

| FP[7:0] BP[7:0] | Front porch period | Back porch period |
|----------------------------|---------------------------|--------------------------|
| 8'h00 | Setting inhibited | Setting inhibited |
| 8'h01 | Setting inhibited | Setting inhibited |
| 8'h02 | Setting inhibited | 2 lines |
| 8'h03 | 3 lines | 3 lines |
| 8'h04 | 4 lines | 4 lines |
| 8'h05 | 5 lines | 5 lines |
| 8'h06 | 6 lines | 6 lines |
| 8'h07 | 7 lines | 7 lines |
| 8'h08 | 8 lines | 8 lines |
| 8'h09 | 9 lines | 9 lines |
| 8'h0A | 10 lines | 10 lines |
| 8'h0B | 11 lines | 11 lines |
| 8'h0C | 12 lines | 12 lines |
| 8'h0D | 13 lines | 13 lines |
| 8'h0E | 14 lines | 14 lines |
| 8'h0F | 15 lines | 15 lines |
| : | : | : |
| 8'h7F | 127 lines | 127 lines |
| 8'h80 | 128 lines | 128 lines |
| 8'h81 | Setting inhibited | Setting inhibited |
| : | : | : |
| 8'hFF | Setting inhibited | Setting inhibited |

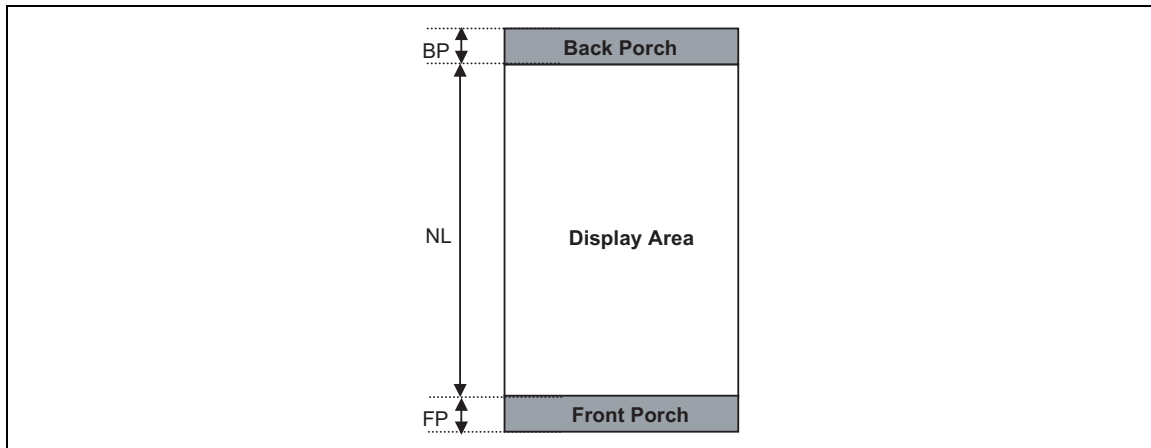


Figure 6 Front and Back Porch Periods

Note to Setting BP and FP

Set the BP and FP bits as follows:

$BP \geq 2$ lines $FP \geq 3$ lines $FP + BP \leq 256$ lines

Make sure the total of lines set by FP and BP is an even number.

Display Control 3 (R09h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------------|------------|------------|-----|-----|-----|-----|------------|------------|------------|------------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | PTS [2] | PTS [1] | PTS [0] | 0 | 0 | PTG | 0 | ISC [3] | ISC [2] | ISC [1] | ISC [0] |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

ISC [3:0]: Set the scan cycle when PTG[1:0] selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

Table 19

| ISC[3:0] | Scan cycle |
|----------|-------------------|
| 4'h0 | Setting inhibited |
| 4'h1 | 3 frames |
| 4'h2 | 5 frames |
| 4'h3 | 7 frames |
| 4'h4 | 9 frames |
| 4'h5 | 11 frames |
| 4'h6 | 13 frames |
| 4'h7 | 15 frames |
| 4'h8 | 17 frames |
| 4'h9 | 19 frames |
| 4'hA | 21 frames |
| 4'hB | 23 frames |
| 4'hC | 25 frames |
| 4'hD | 27 frames |
| 4'hE | 29 frames |
| 4'hF | 31 frames |

PTG: Sets the scan mode in non-display area

Table 20

| PTG | Scan mode in non-display area |
|-----|-------------------------------|
| 0 | Normal scan |
| 1 | Interval scan |

Note: Select frame-inversion AC drive when interval scan is selected.

PTS[2:0]: Sets the source output level in non-display area drive period. When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V31 are halted and the step-up clock

frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

Table 21 Source Output Level and Voltage Generating Operation in Non-display Drive Period

| | PTS[1:0] | Source output level in non lit display area | | Grayscale amplifier operation in non lit display are | Step-up clock frequency in non lit display are |
|---|----------|---|---------------------|--|--|
| | | Positive polarity | Negative polarity | | |
| 0 | 00 | V63 | V0 | V0 to V63 | Register setting (DC0, DC1) |
| | 01 | (Setting inhibited) | (Setting inhibited) | (Setting inhibited) | (Setting inhibited) |
| | 10 | GND | GND | V0 to V63 | Register setting (DC0, DC1) |
| | 11 | Hi-z | Hi-z | V0 to V63 | Register setting (DC0, DC1) |
| 1 | 00 | V63 | V0 | V0, V63 | DC0 setting x 1/2 |
| | 01 | (Setting inhibited) | (Setting inhibited) | (Setting inhibited) | (Setting inhibited) |
| | 10 | GND | GND | V0, V63 | DC0 setting x 1/2 |
| | 11 | Hi-z | Hi-z | V0, V63 | DC0 setting x 1/2 |

Note: Define source polarity in non-lit display area by ND_L bit. Note that if PTS[2]=1, step-up operation may not be executed successfully depending on DC0 and RTN* values.

Display Control 4 (R0Ah)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|--------------|------------|------------|------------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FMARK KOE | FMI [2] | FMI [1] | FMI [0] |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FMI[2:0]: Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE: When FMARKOE = 1, the R61505W starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits. See [“FMARK Interface”](#) for details.

Table 22

| FMI[2] | FMI[1] | FMI[0] | Output interval |
|----------------|--------|--------|------------------|
| 0 | 0 | 0 | 1 frame |
| 0 | 0 | 1 | 2 frames |
| 0 | 1 | 1 | 4 frames |
| 1 | 0 | 1 | 6 frames |
| Other settings | | | Setting disabled |

External Display Interface Control 1 (R0Ch)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------------|------------|------------|------|------|-----|-----|-----|-----|-----------|-----------|-----|-----|------------|------------|
| W | 1 | 0 | ENC [2] | ENC [1] | ENC [0] | 0 | 0 | 0 | RM | 0 | 0 | DM [1] | DM [0] | 0 | 0 | RIM [1] | RIM [0] |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RIM[1:0]: Sets the interface format when RGB interface is selected by RM and DM bits. Set RIM[1:0] bits before starting display operation via RGB interface. Do not change the setting while the R61505W performs display operation.

Table 23 RGB Interface Operation

| RIM[1] | RIM[0] | Bus width | Colors | Used pins |
|--------|--------|---|---------|-------------------|
| 0 | 0 | 18-bit RGB interface (1 transfer/pixel) | 262,144 | DB[17:0] |
| 0 | 1 | 16-bit RGB interface (1 transfer/pixel) | 65,536 | DB[17:13], [11:1] |
| 1 | 0 | Setting inhibited | - | - |
| 1 | 1 | Setting inhibited | - | - |

Note: Instruction bits are set only via system interface.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

Table 24 Display Interface

| DM[1:0] | Display interface |
|---------|---------------------------|
| 2'h0 | Internal clock operations |
| 2'h1 | RGB interface |
| 2'h2 | VSYNC interface |
| 2'h3 | Setting inhibited |

RM: Selects the interface for frame memory access operation. Frame memory access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

Table 25 Frame Memory Access Interface

| RM | Frame memory access interface |
|----|----------------------------------|
| 0 | System interface/VSYNC interface |
| 1 | RGB interface |

ENC[2:0]: Sets the frame memory write cycle via RGB interface.

Table 25 Frame Memory Write Cycle

| ENC[2:0] | Frame Memory Write Cycle (frame periods) |
|----------|---|
| 3'h0 | 1 frame |
| 3'h1 | 2 frames |
| 3'h2 | 3 frames |
| 3'h3 | 4 frames |
| 3'h4 | 5 frames |
| 3'h5 | 6 frames |
| 3'h6 | 7 frames |
| 3'h7 | 8 frames |

Frame Marker Position (R0Dh)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------|-----|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FMP [8] | FMP [7] | FMP [6] | FMP [5] | FMP [4] | FMP [3] | FMP [2] | FMP [1] | FMP [0] |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FMP[8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is outputted at the start of back porch period for 1H period (IOVCC-GND amplitude signal). FMARK can be used as the trigger signal for frame synchronous write operation. See [FMARK Interface](#) for details.

Make sure the setting restriction $9'h000 \leq \text{FMP} \leq \text{BP} + \text{NL} + \text{FP}$.

Table 26

| FMP[8:0] | FMARK output position |
|------------|------------------------|
| 9'h000 | 0 th line |
| 9'h001 | 1 st line |
| 9'h002 | 2 nd line |
| : | : |
| 9'h14E | 334 th line |
| 9'h14F | 335 th line |
| 9'h150~1FF | Setting disabled |

VCOM Low Power Control (R0Eh)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------|-----|-----|-----|-----|------------|------------|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VEM [1] | VEM [0] | 0 | 0 | 0 | 0 |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VEM [1:0]: VCOM equalize function control bit.

When VEM [0]="1", VCOM falls to GND level when switching to VCOMH to VCOML (VCOMH → GND → VCOML).

When VEM [1] = "1", VCOM rises to VCI level when switching to VCOML to VCOMH (VCOML → VCI → VCOMH).

Make sure that $VCI < VCOMH$ and $GND > VCOML$.

Table 27

| VEM[1:0] | Operation |
|----------|---|
| 2'h0 | Normal VCOM drive (No equalizing operation) |
| 2'h1 | Equalize VCOMH (VCOMH→VCOML) |
| 2'h2 | Equalize VCOML (VCOML→VCOMH) |
| 2'h3 | Equalize VCOMH/VCOML |

Note: Check the trade-off between the quality of display on the panel and the power efficiency before use.

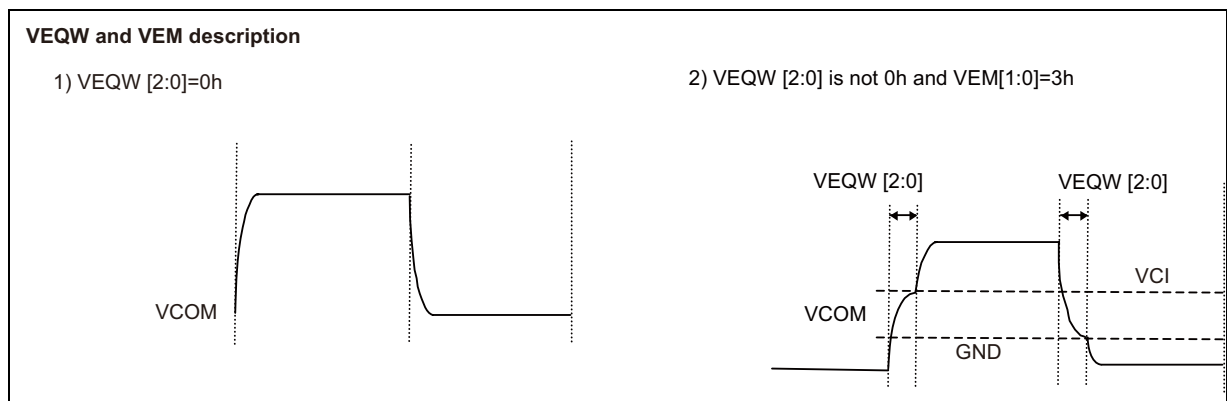


Figure 7

Note: See R93h and R98h for VEQWI and VEQWE descriptions.

External Display Interface Control 2 (R0Fh)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|------|------|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VSPL | HSPL | 0 | EPL | DPL |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DPL: Sets the signal polarity of DOTCLK pin.

DPL = 0: input data on the rising edge of DOTCLK

DPL = 1: input data on the falling edge of DOTCLK

EPL: Sets the signal polarity of ENABLE pin.

EPL = 0: writes data DB17-0 when ENABLE = "0" and disables data write operation when ENABLE = "1".

EPL = 1: writes data DB17-0 when ENABLE = "1" and disables data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of HSYNC pin.

HSPL = 0: low active

HSPL = 1: high active

VSPL: Sets the signal polarity of VSYNC pin.

VSPL = 0: low active

VSPL = 1: high active

Power Control

Power Control 1 (R10h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|-----------|-----------|-----------|-----|-----|-----------|-----------|-----|------|-----|-----|
| W | 1 | 0 | 0 | 0 | 0 | 0 | BT [2] | BT [1] | BT [0] | 0 | 0 | AP [1] | AP [0] | 0 | DSTB | 0 | 0 |
| Default value | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

DSTB: When DSTB = 1, the R61505W enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The frame memory data and instruction setting are not maintained when the R61505W enters the deep standby mode, and they must be reset after exiting deep standby mode.

AP[1:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[1:0] = 2'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

Table 28 Constant Current in Amplifier in LCD Power Supply

| AP[1:0] | LCD power supply circuits |
|---------|---------------------------|
| 2'h0 | Halt operation |
| 2'h1 | 0.5 |
| 2'h2 | 0.75 |
| 2'h3 | 1 |

Note: In this table, the constant current in operational amplifiers is the ratio to the constant current when AP[1:0] is set to 2'h3.

BT[2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

Table 29 Step-up Factor and Output Voltage Level

| BT[2:0] | DDVDH | VCL | VGH | VGL |
|-------------------|-------------------|-----------------|----------------------------|-----------------------------|
| 3'h0 | Setting inhibited | | | |
| 3'h1 | | | | |
| 3'h2 | | | | |
| 3'h3 | VCI1 x2 [x 2] | -VCI1 [x -1] | DDVDH x 3 [x 6] | -(VCI1+DDVDH x 2) [x -5] |
| 3'h4 | | | | -(DDVDH x 2) [x -4] |
| 3'h5 (Default) | | | | -(VCI1+DDVDH) [x -3] |
| 3'h6 | | | VCI1+DDVDH x 2 [x 5] | -(VCI1+DDVDH x 2) [x -5] |
| 3'h7 | | | | -(DDVDH x 2) [x -4] |

- Notes: 1. The step-up factor from VCI1 is shown in the brackets [].
2. Set the following voltages within the respective ranges:
 DDVDH = 6.0V (max.)
 VGH = 18.0V (max.)
 VGL = -13.5V (max.)
 VGH-VGL = 28.0V (max.)
 VCL = -3.0V (max.)

Power Control 2 (R11h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------------|------------|------------|-----|------------|------------|------------|-----|-----------|-----------|-----------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | DC1 [2] | DC1 [1] | DC1 [0] | 0 | DC0 [2] | DC0 [1] | DC0 [0] | 0 | VC [2] | VC [1] | VC [0] |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

DC1[2:0]: Defines step-up clock frequency for the step-up circuit 2. The step-up clock is synchronized with internal clock.

Table 30

| DC1[2:0] | Step-up clock frequency for the step-up circuit 2 (f_{DCDC2}) |
|----------|--|
| 3'h0 | Setting inhibited |
| 3'h1 | Setting inhibited |
| 3'h2 | Line frequency / 4 |
| 3'h3 | Line frequency / 8 |
| 3'h4 | Line frequency / 16 |
| 3'h5 | Setting inhibited |
| 3'h6 | Halt step-up circuit 2 |
| 3'h7 | Setting inhibited |

To calculate step-up clock frequency for the step-up circuit 2

Step-up clock frequency (f_{DCDC2}) = line frequency / $2^{(N)}$ [Hz]

= Clock frequency internal operation f_{osc} / number of clock per line x
division ratio x $2^{(N)}$ [Hz]

f_{osc} : Clock frequency internal operation

Number of clock per line: RTNI [4:0] or RTNE [4:0]

Division ratio: DIVI [1:0] or DIVE [1:0]

N: DC1[2:0] value

DC0[2:0]: Defines step-up clock frequency for the step-up circuit 1. The step-up clock is synchronized with internal clock.

Table 31

| DC0[2:0] | Step-up clock frequency for the step-up circuit 1 (f_{DCDC1}) |
|----------|--|
| 3'h0 | Setting inhibited |
| 3'h1 | Setting inhibited |
| 3'h2 | Setting inhibited |
| 3'h3 | $f_{\text{osc}} / 8$ |
| 3'h4 | $f_{\text{osc}} / 16$ |
| 3'h5 | $f_{\text{osc}} / 32$ |
| 3'h6 | Halt step-up circuit 1 |
| 3'h7 | Setting inhibited |

Note 1: Make sure that $f_{\text{DCDC1}} \geq f_{\text{DCDC2}}$.

Note 2: Make sure to set DC0 and RTN* bits so that

Step-up cycle of the Step-up circuit 1 ≤ 1 line cycle.

Otherwise the step-up operation may fail.

To calculate step-up clock frequency for the step-up circuit 1

Step-up clock frequency (f_{DCDC1}) = Reference clock frequency / 2^N [Hz]

= Clock frequency for internal operation f_{osc} / division ratio $\times 2^N$ [Hz]

f_{osc} : Clock frequency internal operation

Division ratio: DIV1 [1:0] or DIVE [1:0]

N: DC1[2:0] value

VC [2:0]: Defines VCI1 level.

Table 32

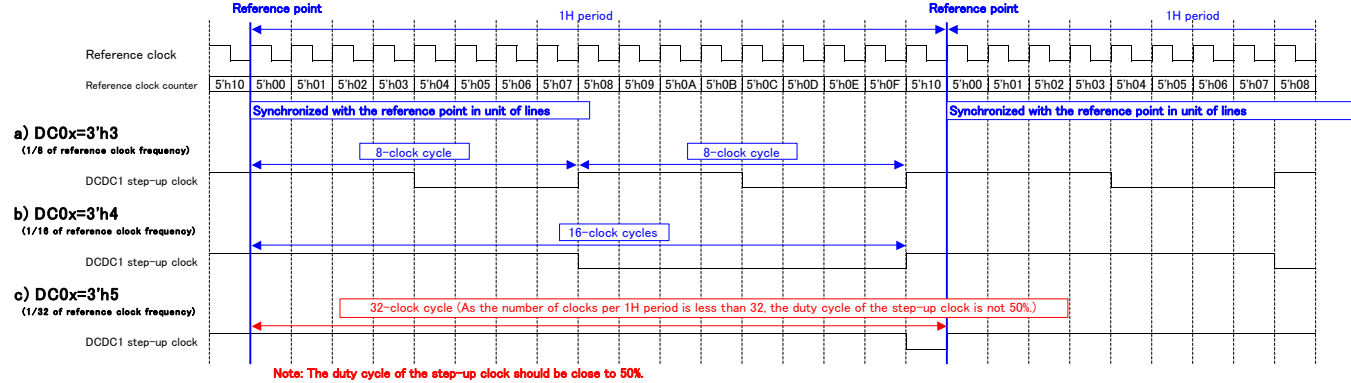
| VC[2:0] | VCI1 (Reference for step-up operation) |
|---------|--|
| 3'h0 | Setting inhibited |
| 3'h1 | 0.94 x VCILVL |
| 3'h2 | 0.89 x VCILVL |
| 3'h3 | Setting inhibited |
| 3'h4 | Setting inhibited |
| 3'h5 | 0.76 x VCIVLV |
| 3'h6 | Setting inhibited |
| 3'h7 | 1.00 x VCILVL |

■ DC0x Value and DCDC1 Step-up Clock Signal Waveform Example

DCDC1 performs charge operation and boost operation with the step-up clock generated from the timing generator.
 The DCDC1 step-up clock frequency is adjusted by setting the division ratio of the reference clock frequency with DC0x register.
 (To prevent flickering, the DCDC1 step-up clock signal is synchronized with the reference point of display operation in unit of lines.)

Note: Set DC0x and RTNI so that (DCDC1 step-up clock frequency) \geq (line clock frequency)
 If the above restriction is not followed, the duty cycle during the boost period is less than 50%. As a result, the step-up circuit may not operate normally.

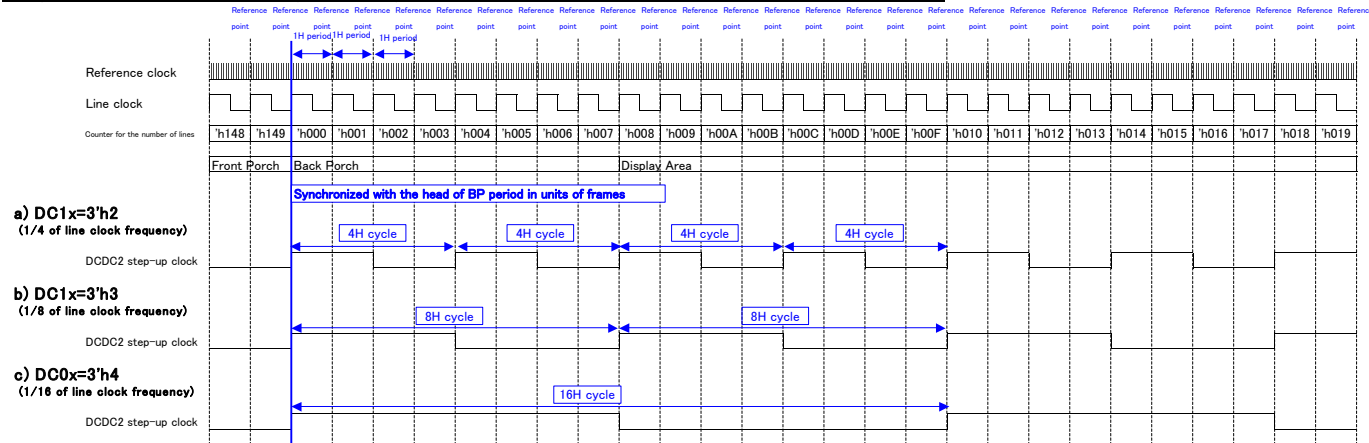
Example) DIVI=2'h1, RTNI=5'h11 (reference clock period = 1/2 of internal operation clock, 1H period = 17 clocks)



■ DC1x Value and DCDC2 Step-up Clock Signal Waveform Example

DCDC2 performs charge operation and boost operation with the step-up clock generated from the timing generator.
 The DCDC2 step-up clock frequency is adjusted by setting the division ratio of the reference clock frequency with DC1x register.
 (To prevent flicker, the DCDC2 step-up clock signal is synchronized with the head of BP period in unit of frames.)

Example) BP=FP=8'h08, NL=7'h4F (front porch = back porch = 8 lines, the number of lines to drive the LCD = 320 lines)



Power Control 3 (R12h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------------|------|------|-----|--------------|-----|-----|----------|-----|------------|------------|------------|------------|
| W | 1 | 0 | 0 | 0 | VRH [0] | 0 | 0 | 0 | VC M R | 1 | 0 | PS ON | PON | VRH [4] | VRH [3] | VRH [2] | VRH [1] |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

VRH[4:0]: Sets the factor to generate VREG1OUT

Table 33

| VRH[4:0] | VREG1OUT |
|-------------|-------------------|
| 5'h00 | Halt (Hi-z) |
| 5'h01-5'h0F | Setting inhibited |
| 5'h10 | VCIR × 1.600 |
| 5'h11 | VCIR × 1.625 |
| 5'h12 | VCIR × 1.650 |
| 5'h13 | VCIR × 1.675 |
| 5'h14 | VCIR × 1.700 |
| 5'h15 | VCIR × 1.725 |
| 5'h16 | VCIR × 1.750 |
| 5'h17 | VCIR × 1.775 |
| 5'h18 | VCIR × 1.800 |
| 5'h19 | VCIR × 1.825 |
| 5'h1A | VCIR × 1.850 |
| 5'h1B | VCIR × 1.875 |
| 5'h1C | VCIR × 1.900 |
| 5'h1D | VCIR × 1.925 |
| 5'h1E | VCIR × 1.950 |
| 5'h1F | VCIR × 1.975 |

Note: Make sure that $VREG1OUT \leq (DDVDH-0.5)V$ in setting VC and VRH bits.

PON, PSON: Turns power supply on. Write PON and PSON to turn power supply on. Internal power supply operation starts. Follow the Power On sequences.

Table 34 Power supply sequences (PSON, PON)

| PSON | PON | Operation |
|------|-----|---------------------------|
| 0 | 0 | Power supply OFF sequence |
| 0 | 1 | Power supply OFF sequence |
| 1 | 0 | Power supply OFF sequence |
| 1 | 1 | Power supply ON sequence |

VCMR: Select VCOMH voltage level from external resistance (VCOMR), internal electronic volumes VCM1 and VCM2.

Table 35

| VCMR | VCOMH level |
|-------------|----------------------------|
| 0 | VCOMR |
| 1 (Default) | Internal electronic volume |

Note: Internal electronic volume is adjusted by VCM1 and VCM2 bits.

Power Control 4 (R13h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------------|------------|------------|------------|------------|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | VDV [4] | VDV [3] | VDV [2] | VDV [1] | VDV [0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDV[4:0]: Set VCOM alternating amplitude in the range of VREG1OUTx0.70 to VREG1OUTx1.32.

Table 36 VDV Setting

| VDV[4:0] | VCOM Amplitude | VDV[4:0] | VCOM Amplitude |
|----------|----------------|----------|----------------|
| 5'h0 | VREG1OUT×0.70 | 5'h10 | VREG1OUT×1.02 |
| 5'h1 | VREG1OUT×0.72 | 5'h11 | VREG1OUT×1.04 |
| 5'h2 | VREG1OUT×0.74 | 5'h12 | VREG1OUT×1.06 |
| 5'h3 | VREG1OUT×0.76 | 5'h13 | VREG1OUT×1.08 |
| 5'h4 | VREG1OUT×0.78 | 5'h14 | VREG1OUT×1.10 |
| 5'h5 | VREG1OUT×0.80 | 5'h15 | VREG1OUT×1.12 |
| 5'h6 | VREG1OUT×0.82 | 5'h16 | VREG1OUT×1.14 |
| 5'h7 | VREG1OUT×0.84 | 5'h17 | VREG1OUT×1.16 |
| 5'h8 | VREG1OUT×0.86 | 5'h18 | VREG1OUT×1.18 |
| 5'h9 | VREG1OUT×0.88 | 5'h19 | VREG1OUT×1.20 |
| 5'hA | VREG1OUT×0.90 | 5'h1A | VREG1OUT×1.22 |
| 5'hB | VREG1OUT×0.92 | 5'h1B | VREG1OUT×1.24 |
| 5'hC | VREG1OUT×0.94 | 5'h1C | VREG1OUT×1.26 |
| 5'hD | VREG1OUT×0.96 | 5'h1D | VREG1OUT×1.28 |
| 5'hE | VREG1OUT×0.98 | 5'h1E | VREG1OUT×1.30 |
| 5'hF | VREG1OUT×1.00 | 5'h1F | VREG1OUT×1.32 |

Note: Set VDV[4:0] so that VCOM amplitude becomes 6.0V or smaller.

Frame Memory Access Control

Frame Memory Address Set (Horizontal Address) (R20h)

Frame Memory Address Set (Vertical Address) (R21h)

| | R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------|---------------|----|------|------|------|------|------|------|-----|------------|------------|------------|------------|------------|------------|------------|-----------|-----------|
| R 20 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | AD [7] | AD [6] | AD [5] | AD [4] | AD [3] | AD [2] | AD [1] | AD [0] |
| | Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 21 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | AD [16] | AD [15] | AD [14] | AD [13] | AD [12] | AD [11] | AD [10] | AD [9] | AD [8] |
| | Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

AD[16:0]: A frame memory address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the R61505W writes data to the internal frame memory so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal frame memory.

- Notes:
1. In RGB interface operation (RM = "1"), the address AD[16:0] is set in the address counter every frame on the falling edge of VSYNC.
 2. In internal clock operation and VSYNC interface operation (RM = "0"), the address AD[16:0] is set when executing the instruction.

Table 37 Frame Memory Address Setting Range

| AD[16:0] | Frame memory data setting |
|-----------------------|---|
| 17'h00000 – 17'h000EF | Bitmap data on the 1 st line |
| 17'h00100 – 17'h001EF | Bitmap data on the 2 nd line |
| 17'h00200 – 17'h002EF | Bitmap data on the 3 rd line |
| 17'h00300 – 17'h003EF | Bitmap data on the 4 th line |
| 17'h00400 – 17'h004EF | Bitmap data on the 5 th line |
| : | : |
| 17'h13C00 – 17'h13CEF | Bitmap data on the 317 th line |
| 17'h13D00 – 17'h13DEF | Bitmap data on the 318 th line |
| 17'h13E00 – 17'h13EEF | Bitmap data on the 319 th line |
| 17'h13F00 – 17'h13FEF | Bitmap data on the 320 th line |

Frame Memory Data Write (R22h)

R/W RS

| | | |
|-------------------|---|---|
| W | 1 | Frame memory write data WD[17:0] is transferred via different data bus in different interface operations. |
| RGB I/F operation | | Frame memory write data WD[17:0] is transferred via different data bus in different interface operations. |

WD[17:0]: The R61505W develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation.

The frame memory data represents the grayscale level. The R61505W automatically updates the address according to AM and I/D[1:0] settings as it writes data in the frame memory. The DFM bit sets the format to develop 16-bit data into the 18-bit data in 16-bit or 8-bit interface operation.

Note: When writing data in the frame memory via system interface while using the RGB interface, make sure that write operations via two interfaces do not conflict one another.

Frame Memory Data Read (R22h)

R/W RS

| | | |
|---|---|--|
| R | 1 | Frame memory read data RD[17:0] is transferred via different data bus in different interface operations. |
|---|---|--|

RD[17:0]: 18-bit data read from the frame memory. Frame memory read data RD[17:0] is transferred via different data bus in different interface operation.

When the R61505W reads data from the frame memory to the host processor, the first word read immediately after frame memory address set is not outputted, so that it is invalid. Valid data is sent to the data bus when the R61505W reads out the second and subsequent words.

When either 8-bit or 16-bit interface is selected, the LSBs of R dot data and B dot data are not read out.

Note: This register is disabled in RGB interface operation.

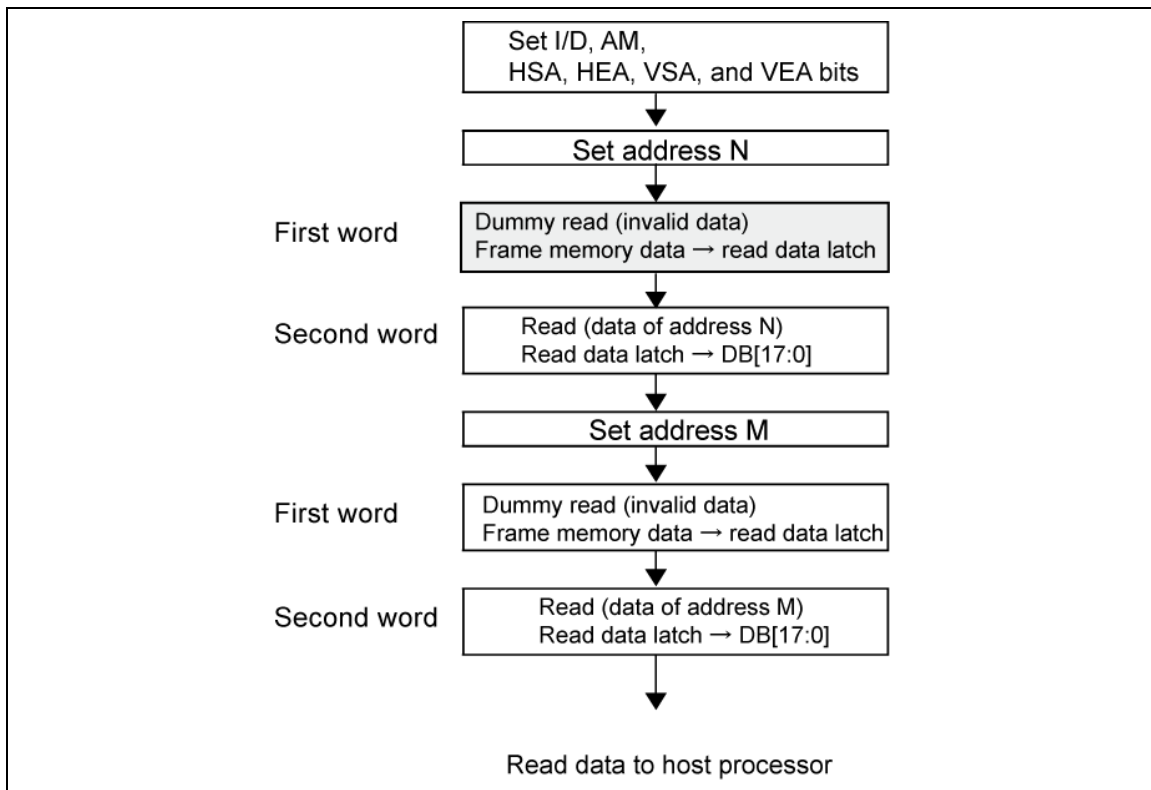


Figure 8 Frame Memory Read Sequence

NVM Write Control

NVM Data Read 1 (R28), NVM Data Read 2 (R29h), NVM Data Read 3 (R2Ah)

| | R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|---------|----|------|------|------|------|------|------|-----|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------|
| R28 | R/W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | UID [7] | UID [6] | UID [5] | UID [4] | UID [3] | UID [2] | UID [1] | UID [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R29 | R/W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VC M1 [6] | VC M1 [5] | VC M1 [4] | VC M1 [3] | VC M1 [2] | VC M1 [1] | VC M1 [0] | |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R2A | R/W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VC MSE L | VC M2 [6] | VC M2 [5] | VC M2 [4] | VC M2 [3] | VC M2 [2] | VC M2 [1] | VC M2 [0] | |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

UID[7:0]: The data bits UID[7:0] are written to the designated address in NVM and the written data can be read out from NVM by instruction setting (CALB) to this register. UID[7:0] can be used to write and read user identification code in NVM.

The setting value in UID[7:0] bits is enabled when not reading out the setting value from NVM via CALB setting.

VCM1[6:0]: Selects the factor of VREG1OUT to generate VCOMH. When enabling the setting valued in VCM1[6:0], make sure to set VCMSEL = 1.

When using the data written in NVM for setting the VCOMH level, the data bits VCM1[6:0] are written to the designated address in NVM and the written data can be read out from NVM by instruction setting (CALB) to this register. When the data bits VCM2[6:0] are written in NVM before writing the data bits VCM1[6:0] to NVM, the VCM1[6:0] setting value written in NVM cannot be used for setting the VCOMH level.

VCM2[6:0]: Selects the factor of VREG1OUT to generate VCOMH. When enabling the setting valued in VCM2[6:0], make sure to set VCMSEL = 0. The function of VCM2[6:0] instruction is the same as that of VCM1[6:0].

Write the setting value in VCM2[6:0] bits and VCMSEL = 0 in the designated addresses of NVM, when reading out the setting value written in NVM for VCOMH level setting and the data is already written in the designated address of VCM1[6:0] in the NVM. The VCM2[6:0] data bits written in NVM can be read out via CALB setting for setting the VCOMH level.

Note: When R2A register is read after setting CALB=1 (RA4h), data in IB6-5, R2Ah, is not always 0 and different data may be read out from different die.

VCMSEL: When VCMSEL = 1, VCM1 is selected. When VCMSEL = 0, VCM2 is selected.

Table 38

| VCM1[6:0] VCM2[6:0] | VCOMH | VCM1[6:0] VCM2[6:0] | VCOMH | VCM1[6:0] VCM2[6:0] | VCOMH |
|------------------------|------------------|------------------------|------------------|------------------------|------------------|
| 7'h 00 | VREG1OUT X 0.492 | 7'h2B | VREG1OUT X 0.664 | 7'h56 | VREG1OUT X 0.836 |
| 7'h 01 | VREG1OUT X 0.496 | 7'h2C | VREG1OUT X 0.668 | 7'h57 | VREG1OUT X 0.840 |
| 7'h 02 | VREG1OUT X 0.500 | 7'h2D | VREG1OUT X 0.672 | 7'h58 | VREG1OUT X 0.844 |
| 7'h03 | VREG1OUT X 0.504 | 7'h2E | VREG1OUT X 0.676 | 7'h59 | VREG1OUT X 0.848 |
| 7'h04 | VREG1OUT X 0.508 | 7'h2F | VREG1OUT X 0.680 | 7'h5A | VREG1OUT X 0.852 |
| 7'h05 | VREG1OUT X 0.512 | 7'h30 | VREG1OUT X 0.684 | 7'h5B | VREG1OUT X 0.856 |
| 7'h06 | VREG1OUT X 0.516 | 7'h31 | VREG1OUT X 0.688 | 7'h5C | VREG1OUT X 0.860 |
| 7'h07 | VREG1OUT X 0.520 | 7'h32 | VREG1OUT X 0.692 | 7'h5D | VREG1OUT X 0.864 |
| 7'h08 | VREG1OUT X 0.524 | 7'h33 | VREG1OUT X 0.696 | 7'h5E | VREG1OUT X 0.868 |
| 7'h09 | VREG1OUT X 0.528 | 7'h34 | VREG1OUT X 0.700 | 7'h5F | VREG1OUT X 0.872 |
| 7'h0A | VREG1OUT X 0.532 | 7'h35 | VREG1OUT X 0.704 | 7'h60 | VREG1OUT X 0.876 |
| 7'h0B | VREG1OUT X 0.536 | 7'h36 | VREG1OUT X 0.708 | 7'h61 | VREG1OUT X 0.880 |
| 7'h0C | VREG1OUT X 0.540 | 7'h37 | VREG1OUT X 0.712 | 7'h62 | VREG1OUT X 0.884 |
| 7'h0D | VREG1OUT X 0.544 | 7'h38 | VREG1OUT X 0.716 | 7'h63 | VREG1OUT X 0.888 |
| 7'h0E | VREG1OUT X 0.548 | 7'h39 | VREG1OUT X 0.720 | 7'h64 | VREG1OUT X 0.892 |
| 7'h0F | VREG1OUT X 0.552 | 7'h3A | VREG1OUT X 0.724 | 7'h65 | VREG1OUT X 0.896 |
| 7'h10 | VREG1OUT X 0.556 | 7'h3B | VREG1OUT X 0.728 | 7'h66 | VREG1OUT X 0.900 |
| 7'h11 | VREG1OUT X 0.560 | 7'h3C | VREG1OUT X 0.732 | 7'h67 | VREG1OUT X 0.904 |
| 7'h12 | VREG1OUT X 0.564 | 7'h3D | VREG1OUT X 0.736 | 7'h68 | VREG1OUT X 0.908 |
| 7'h13 | VREG1OUT X 0.568 | 7'h3E | VREG1OUT X 0.740 | 7'h69 | VREG1OUT X 0.912 |
| 7'h14 | VREG1OUT X 0.572 | 7'h3F | VREG1OUT X 0.744 | 7'h6A | VREG1OUT X 0.916 |
| 7'h15 | VREG1OUT X 0.576 | 7'h40 | VREG1OUT X 0.748 | 7'h6B | VREG1OUT X 0.920 |
| 7'h16 | VREG1OUT X 0.580 | 7'h41 | VREG1OUT X 0.752 | 7'h6C | VREG1OUT X 0.924 |
| 7'h17 | VREG1OUT X 0.584 | 7'h42 | VREG1OUT X 0.756 | 7'h6D | VREG1OUT X 0.928 |
| 7'h18 | VREG1OUT X 0.588 | 7'h43 | VREG1OUT X 0.760 | 7'h6E | VREG1OUT X 0.932 |
| 7'h19 | VREG1OUT X 0.592 | 7'h44 | VREG1OUT X 0.764 | 7'h6F | VREG1OUT X 0.936 |
| 7'h1A | VREG1OUT X 0.596 | 7'h45 | VREG1OUT X 0.768 | 7'h70 | VREG1OUT X 0.940 |
| 7'h1B | VREG1OUT X 0.600 | 7'h46 | VREG1OUT X 0.772 | 7'h71 | VREG1OUT X 0.944 |
| 7'h1C | VREG1OUT X 0.604 | 7'h47 | VREG1OUT X 0.776 | 7'h72 | VREG1OUT X 0.948 |
| 7'h1D | VREG1OUT X 0.608 | 7'h48 | VREG1OUT X 0.780 | 7'h73 | VREG1OUT X 0.952 |
| 7'h1E | VREG1OUT X 0.612 | 7'h49 | VREG1OUT X 0.784 | 7'h74 | VREG1OUT X 0.956 |
| 7'h1F | VREG1OUT X 0.616 | 7'h4A | VREG1OUT X 0.788 | 7'h75 | VREG1OUT X 0.960 |
| 7'h20 | VREG1OUT X 0.620 | 7'h4B | VREG1OUT X 0.792 | 7'h76 | VREG1OUT X 0.964 |
| 7'h21 | VREG1OUT X 0.624 | 7'h4C | VREG1OUT X 0.796 | 7'h77 | VREG1OUT X 0.968 |
| 7'h22 | VREG1OUT X 0.628 | 7'h4D | VREG1OUT X 0.800 | 7'h78 | VREG1OUT X 0.972 |
| 7'h23 | VREG1OUT X 0.632 | 7'h4E | VREG1OUT X 0.804 | 7'h79 | VREG1OUT X 0.976 |
| 7'h24 | VREG1OUT X 0.636 | 7'h4F | VREG1OUT X 0.808 | 7'h7A | VREG1OUT X 0.980 |
| 7'h25 | VREG1OUT X 0.640 | 7'h50 | VREG1OUT X 0.812 | 7'h7B | VREG1OUT X 0.984 |
| 7'h26 | VREG1OUT X 0.644 | 7'h51 | VREG1OUT X 0.816 | 7'h7C | VREG1OUT X 0.988 |
| 7'h27 | VREG1OUT X 0.648 | 7'h52 | VREG1OUT X 0.820 | 7'h7D | VREG1OUT X 0.992 |
| 7'h28 | VREG1OUT X 0.652 | 7'h53 | VREG1OUT X 0.824 | 7'h7E | VREG1OUT X 0.996 |
| 7'h29 | VREG1OUT X 0.656 | 7'h54 | VREG1OUT X 0.828 | 7'h7F | VREG1OUT X 1.000 |
| 7'h2A | VREG1OUT X 0.660 | 7'h55 | VREG1OUT X 0.832 | | |

γ Control γ Control 1 ~ 10 (R30h ~ R39h)

| | | IB | | | | | | | | | | | | | | | | |
|---------|---------|------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|---|-----|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | 6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 | |
| R 30 | W | 1 | 0 | 0 | 0 | PR0 P01 [4] | PR0 P01 [3] | PR0 P01 [2] | PR0 P01 [1] | PR0 P01 [0] | 0 | 0 | 0 | PR0 P00 [4] | PR0 P00 [3] | PR0 P00 [2] | PR0 P00 [1] | PR0 P00 [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 31 | W | 1 | PR0 P04 [3] | PR0 P04 [2] | PR0 P04 [1] | PR0 P04 [0] | PR0 P03 [3] | PR0 P03 [2] | PR0 P03 [1] | PR0 P03 [0] | 0 | 0 | 0 | PR0 P02 [4] | PR0 P02 [3] | PR0 P02 [2] | PR0 P02 [1] | PR0 P02 [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 32 | W | 1 | 0 | 0 | 0 | PR0 P06 [4] | PR0 P06 [3] | PR0 P06 [2] | PR0 P06 [1] | PR0 P06 [0] | 0 | 0 | 0 | PR0P 05 [3] | PR0P 05 [2] | PR0 P05 [1] | PR0 P05 [0] | |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 33 | W | 1 | 0 | 0 | 0 | PR0 P08 [4] | PR0 P08 [3] | PR0 P08 [2] | PR0 P08 [1] | PR0 P08 [0] | 0 | 0 | 0 | PR0 P07 [4] | PR0 P07 [3] | PR0 P07 [2] | PR0 P07 [1] | PR0 P07 [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 34 | W | 1 | 0 | 0 | PI0 P3 [1] | PI0 P3 [0] | 0 | 0 | PI0 P2 [1] | PI0 P2 [0] | 0 | 0 | PI0 P1 [1] | PI0 P1 [0] | 0 | 0 | PI0 P0 [1] | PI0 P0 [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 35 | W | 1 | 0 | 0 | 0 | PR0 N01 [4] | PR0 N01 [3] | PR0 N01 [2] | PR0 N01 [1] | PR0 N01 [0] | 0 | 0 | 0 | PR0 N00 [4] | PR0 N00 [3] | PR0 N00 [2] | PR0 N00 [1] | PR0 N00 [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 36 | W | 1 | PR0 N04 [3] | PR0 N04 [2] | PR0 N04 [1] | PR0 N04 [0] | PR0 N03 [3] | PR0 N03 [2] | PR0 N03 [1] | PR0 N03 [0] | 0 | 0 | 0 | PR0 N02 [4] | PR0 N02 [3] | PR0 N02 [2] | PR0 N02 [1] | PR0 N02 [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 37 | W | 1 | 0 | 0 | 0 | PR0 N06 [4] | PR0 N06 [3] | PR0 N06 [2] | PR0 N06 [1] | PR0 N06 [0] | 0 | 0 | 0 | PR0 N05 [3] | PR0 N05 [2] | PR0 N05 [1] | PR0 N05 [0] | |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 38 | W | 1 | 0 | 0 | 0 | PR0 N08 [4] | PR0 N08 [3] | PR0 N08 [2] | PR0 N08 [1] | PR0 N08 [0] | 0 | 0 | 0 | PR0 N07 [4] | PR0 N07 [3] | PR0 N07 [2] | PR0 N07 [1] | PR0 N07 [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 39 | W | 1 | 0 | 0 | PI0 N3 [1] | PI0 N3 [0] | 0 | 0 | PI0 N2 [1] | PI0 N2 [0] | 0 | 0 | PI0 N1 [1] | PI0 N1 [0] | 0 | 0 | PI0 N0 [1] | PI0 N0 [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- PR0P00[4:0] R0 reference level adjustment register for positive polarity
 PR0N00[4:0] R0 reference level adjustment register for negative polarity
 PR0P01[4:0] R1 reference level adjustment register for positive polarity
 PR0N01[4:0] R1 reference level adjustment register for negative polarity
 PR0P02[4:0] R2 reference level adjustment register for positive polarity
 PR0N02[4:0] R2 reference level adjustment register for negative polarity

| | |
|--------------|---|
| PR0P03[3:0] | R3 reference level adjustment register for positive polarity |
| PR0N03[3:0] | R3 reference level adjustment register for negative polarity |
| PR0P04[3:0] | R4 reference level adjustment register for positive polarity |
| PR0N04[3:0] | R4 reference level adjustment register for negative polarity |
| PR0P05[3:0] | R5 reference level adjustment register for positive polarity |
| PR0N05[3:0] | R5 reference level adjustment register for negative polarity |
| PR0P06[4:0] | R6 reference level adjustment register for positive polarity |
| PR0N06[4:0] | R6 reference level adjustment register for negative polarity |
| PR0P07[4:0] | R7 reference level adjustment register for positive polarity |
| PR0N07[4:0] | R7 reference level adjustment register for negative polarity |
| PR0P08[4:0] | R8 reference level adjustment register for positive polarity |
| PR0N08[4:0] | R8 reference level adjustment register for negative polarity |
| PI0P0~1[1:0] | Interpolation adjustment register for positive polarity (V2~V7) |
| PI0N0~1[1:0] | Interpolation adjustment register for negative polarity (V2~V7) |
| PI0P2~3[1:0] | Interpolation adjustment register for positive polarity (V56~61) |
| PI0N2~3[1:0] | Interpolation adjustment register for negative polarity (V56~V61) |

Window Address Control**Window Horizontal Frame Memory Address (Start Address) (R50h)****Window Horizontal Frame Memory Address (End Address) (R51h)****Window Vertical Frame Memory Address (Start Address) (R52h)****Window Vertical Frame Memory Address (End Address) (R53h)**

| | R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------|---------|----|------|------|------|------|------|------|-----|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| R 50 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HSA [7] | HSA [6] | HSA [5] | HSA [4] | HSA [3] | HSA [2] | HSA [1] | HSA [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 51 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HEA [7] | HEA [6] | HEA [5] | HEA [4] | HEA [3] | HEA [2] | HEA [1] | HEA [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| R 52 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VSA [8] | VSA [7] | VSA [6] | VSA [5] | VSA [4] | VSA [3] | VSA [2] | VSA [1] | VSA [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 53 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VEA [8] | VEA [7] | VEA [6] | VEA [5] | VEA [4] | VEA [3] | VEA [2] | VEA [1] | VEA [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

HSA[7:0], HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting frame memory write operation. In setting, make sure that $8'h00 \leq HSA < HEA \leq 8'hEF$ and $8'h04 \leq HEA - HSA$.

VSA[8:0], VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting frame memory write operation. In setting, make sure that $9'h000 \leq VSA < VEA \leq 9'h13F$.

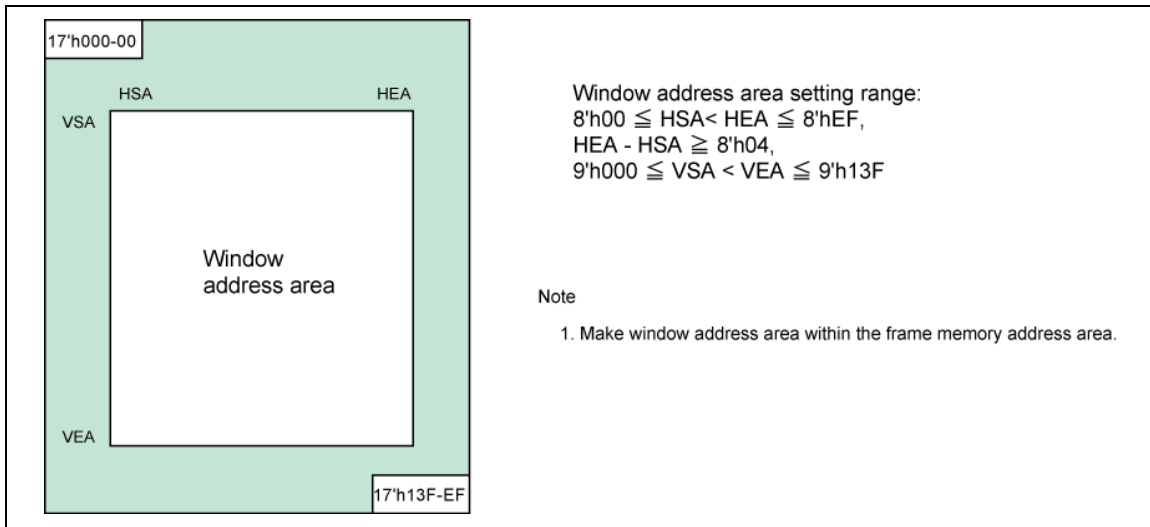


Figure 9 Frame Memory Address Map and Window Address Area

Base Image Display Control**Driver Output Control (R60h),****Base Image Display Control (R61h)****Vertical Scroll Control (R6Ah)**

| | R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|---------|----|------|------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|------------|------------|------------|------------|------------|------------|
| R60 | W | 1 | GS | 0 | NL [5] | NL [4] | NL [3] | NL [2] | NL [1] | NL [0] | 0 | 0 | SCN [5] | SCN [4] | SCN [3] | SCN [2] | SCN [1] | SCN [0] |
| | Default | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R61 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NDL | VLE | REV |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R6A | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VL [8] | VL [7] | VL [6] | VL [5] | VL [4] | VL [3] | VL [2] | VL [1] | VL [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The frame memory address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 39

| NL[5:0] | Number of drive lines |
|----------------|------------------------------|
| 6'h00-6'h1C | Setting inhibited |
| 6'h1D | 240 lines |
| 6'h1E | 248 lines |
| 6'h1F | 256 lines |
| 6'h20 | 264 lines |
| 6'h21 | 272 lines |
| 6'h22 | 280 lines |
| 6'h23 | 288 lines |
| 6'h24 | 296 lines |
| 6'h25 | 304 lines |
| 6'h26 | 312 lines |
| 6'h27 | 320 lines |
| 6'h28-6'h3F | Setting inhibited |

GS: Sets the direction of scan by the gate driver. Set GS bit in combination with SM and SS bits for the convenience of the display module configuration and the display direction.

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the R61505W to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

Table 40 Frame Memory Data Grayscale Level Inversion

| REV | Frame memory data | Source output level in display area | |
|-----|-------------------|-------------------------------------|-------------------|
| | | Positive polarity | Negative polarity |
| 0 | 18'h00000 | V63 | V0 |
| | : | : | : |
| | 18'h3FFFF | V0 | V63 |
| 1 | 18'h00000 | V0 | V63 |
| | : | : | : |
| | 18'h3FFFF | V63 | V0 |

VLE: Vertical scroll display enable bit. When VLE = 1, the R61505W starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

Table 41

| VLE | Base image |
|-----|------------------|
| 0 | Fixed |
| 1 | Enable scrolling |

NDL: Sets the source output level in non-lit display area. NDL bit can keep the non-display area lit on.

Table 42

| NDL | Non-display area | |
|-----|------------------|----------|
| | Positive | Negative |
| 0 | V63 | V0 |
| 1 | V0 | V63 |

VL[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[8:0]. Make sure $VL[8:0] \leq 320$.

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

Table 43

| SCN[5:0] | Gate line No (Scan start position) | | | |
|-------------|------------------------------------|-------------------|-------------------|-------------------|
| | SM=0 | | SM=1 | |
| | GS=0 | GS=1 | GS=0 | GS=1 |
| 6'h00 | G1 | G(N) | G1 | G(2N-320) |
| 6'h01 | G9 | G(N+8) | G16 | G(2N-304) |
| 6'h02 | G17 | G(N+16) | G33 | G(2N-288) |
| 6'h03 | G25 | G(N+24) | G49 | G(2N-272) |
| 6'h04 | G33 | G(N+32) | G65 | G(2N-256) |
| 6'h05 | G41 | G(N+40) | G81 | G(2N-240) |
| 6'h06 | G49 | G(N+48) | G97 | G(2N-224) |
| 6'h07 | G57 | G(N+56) | G113 | G(2N-208) |
| 6'h08 | G65 | G(N+64) | G129 | G(2N-192) |
| 6'h09 | G73 | G(N+72) | G145 | G(2N-176) |
| 6'h0A | G81 | G(N+80) | G161 | G(2N-160) |
| 6'h0B-6'h2F | Setting inhibited | Setting inhibited | Setting inhibited | Setting inhibited |

Note: N means the number of lines set by register.

When setting the SCN bit, make sure to satisfy the restriction below:

Table 44

| SM | GS | Restriction |
|----|----|--|
| 0 | 0 | (Scan start position-1) + (Number of line (NL bit)) ≤ 320 |
| 0 | 1 | Scan start position ≤ 320 |
| 1 | 0 | (Scan start position -1)/2 + (Number of line (NL bit)) ≤ 320 |
| 1 | 1 | Scan start position ≤ 320 |

Partial Display Control**Partial Image Display Position (R80h)****Partial Image Frame Memory Address (Start Line Address) (R81h)****Partial Image Frame Memory Address (End Line Address) (R82h)**

| | R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------|---------------|----|------|------|------|------|------|------|-----|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| R 80 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PTDP [8] | PTDP [7] | PTDP [6] | PTDP [5] | PTDP [4] | PTDP [3] | PTDP [2] | PTDP [1] | PTDP [0] |
| | Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 81 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PTSA [8] | PTSA [7] | PTSA [6] | PTSA [5] | PTSA [4] | PTSA [3] | PTSA [2] | PTSA [1] | PTSA [0] |
| | Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R 82 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PTE A[8] | PTE A[7] | PTE A[6] | PTE A[5] | PTE A[4] | PTE A[3] | PTE A[2] | PTE A[1] | PTE A[0] |
| | Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PTDP[8:0]: Sets the display position of partial image.

If PTDP0 = “9’h000”, the partial image is displayed from the first line of the base image.

PTSA[8:0], PTEA[8:0]: Sets the start line and end line addresses of the frame memory area, respectively for the partial image. In setting, make sure that $PTSA \leq PTEA$.

Panel Interface Control

Panel Interface Control 1 (R90h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------|-------------|-------------|-----|-----|-----|-------------|-------------|-------------|-------------|-------------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | DIVI [1] | DIVI [0] | 0 | 0 | 0 | RTNI [4] | RTNI [3] | RTNI [2] | RTNI [1] | RTNI [0] |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

RTNI[4:0]: Sets 1H (line) period. This setting is enabled while the R61505W's display operation is synchronized with internal clock.

Table 45 Clocks per Line (Internal Clock Operation: 1 clock = 1 OSC)

| RTNI[4:0] | Clocks per line | RTNI[4:0] | Clocks per line | RTNI[4:0] | Clocks per line |
|-------------|-------------------|-----------|-----------------|-----------|-----------------|
| 5'h00-5'h0F | Setting inhibited | 5'h15 | 21 clocks | 5'h1B | 27 clocks |
| 5'h10 | 16 clocks | 5'h16 | 22 clocks | 5'h1C | 28 clocks |
| 5'h11 | 17 clocks | 5'h17 | 23 clocks | 5'h1D | 29 clocks |
| 5'h12 | 18 clocks | 5'h18 | 24 clocks | 5'h1E | 30 clocks |
| 5'h13 | 19 clocks | 5'h19 | 25 clocks | 5'h1F | 31 clocks |
| 5'h14 | 20 clocks | 5'h1A | 26 clocks | | |

Note: In Power Supply Instruction Setting, Deep Standby Exit Sequence and Sleep Mode Exit Sequence, RTNI bit must be set at the "Initial instruction setting" stage.

DIVI[1:0]: Sets the division ratio of the internal clock frequency. The R61505W's internal operation is synchronized with the frequency divided internal clock. When DIVI[1:0] setting is changed, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too. For details, see "Frame Frequency Adjustment Function".

The setting in DIVI[1:0] is disabled in RGB interface operation. Setting $DIVI \neq 2'h0$ is inhibited.

Table 46 Division Ratio of the Internal Clock

| DIVI[1:0] | Division Ratio |
|-----------|----------------|
| 2'h0 | 1/1 |
| 2'h1 | 1/2 |
| 2'h2 | 1/4 |
| 2'h3 | 1/8 |

Note: In Power Supply Instruction Setting, Deep Standby Exit Sequence and Sleep Mode Exit Sequence, DIVI bit must be set at the "Initial instruction setting" stage.

Frame Frequency Calculation

| |
|---|
| $\text{Frame frequency} = \frac{f_{osc}}{\text{Clocks per line} \times \text{division ratio} \times (\text{line} + \text{BP} + \text{FP})} \quad [\text{Hz}]$ <p> <i>f_{osc}</i> : Internal oscillation frequency Line: Number of lines to drive the LCD (NL bits) Division ratio: DIVI Clocks per line: RTNI </p> |
|---|

Panel Interface Control 1-1 (R91h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|--------------|--------------|--------------|--------------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SPC WI[3] | SPC WI[2] | SPC WI[1] | SPC WI[0] |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

SPCWI [3:0]: The bit is used to set source VCI precharge period. Precharge period is set by SPCWI[3:0] starting from the source output alternating position defined by SDTI[2:0]. This bit is disabled when RGB interface is selected.

Table 47

SPCWI [3:0] Source VCI precharge period

| | |
|------|-----------|
| 4'h0 | 0 clocks |
| 4'h1 | 1 clock |
| 4'h2 | 2 clocks |
| 4'h3 | 3 clocks |
| 4'h4 | 4 clocks |
| 4'h5 | 5 clocks |
| 4'h6 | 6 clocks |
| 4'h7 | 7 clocks |
| 4'h8 | 8 clocks |
| 4'h9 | 9 clocks |
| 4'hA | 10 clocks |
| 4'hB | 11 clocks |
| 4'hC | 12 clocks |
| 4'hD | 13 clocks |
| 4'hE | 14 clocks |
| 4'hF | 15 clocks |

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVI (R90h).

Panel Interface Control 2(R92h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|-------------|-------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | 0 | 0 | NOW I[2] | NOW I[1] | NOW I[0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

NOWI[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation synchronizing with the internal clock.

Table 48

| NOWI[2:0] | Non-overlap period | NOWI[2:0] | Non-overlap period |
|------------------|---------------------------|------------------|---------------------------|
| 3'h0 | Setting inhibited | 3'h4 | 4 clocks |
| 3'h1 | 1 clock | 3'h5 | 5 clocks |
| 3'h2 | 2 clocks | 3'h6 | 6 clocks |
| 3'h3 | 3 clocks | 3'h7 | 7 clocks |

Note: The internal clock is the frequency divided clock, which is set by DIVI (R90h) bits.

Panel Interface Control 3(R93h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|-----------|-----------|-----------|-----|-----|-----|-----|-----|----------|----------|----------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | VEQWI [2] | VEQWI [1] | VEQWI [0] | 0 | 0 | 0 | 0 | 0 | MCP I[2] | MCP I[1] | MCP I[0] |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

VEQWI [2:0]: Sets VCOM equalize period. Equalizing operation continues for the period defined by VEQWI bit starting from the VCOM alternating position defined by MCPI [2:0]. VEQWI setting is enabled when VEM[1:0]=1 or larger (R0Eh) and display operation of the R61505W is synchronized with internal clock.

VEQWI is disabled when RGB interface is selected.

Table 49

VEQWI[2:0] VCOM equalize period

| | |
|------|----------|
| 3'h0 | 0 clocks |
| 3'h1 | 1 clock |
| 3'h2 | 2 clocks |
| 3'h3 | 3 clocks |
| 3'h4 | 4 clocks |
| 3'h5 | 5 clocks |
| 3'h6 | 6 clocks |
| 3'h7 | 7 clocks |

Note: DIVI (R90h) sets division ratio of clock frequency.

MCPI[2:0]: Sets the source output timing by the number of internal clock from the reference point. The setting is enabled display operation of the R61505W is synchronized with internal clock.

MCPI is disabled when RGN interface is selected.

Table 50

| MCPI[2:0] | Source output position | MCPI[2:0] | Source output position |
|-----------|------------------------|-----------|------------------------|
| 3'h0 | Setting inhibited | 3'h4 | 4 clocks |
| 3'h1 | 1 clock | 3'h5 | 5 clocks |
| 3'h2 | 2 clocks | 3'h6 | 6 clocks |
| 3'h3 | 3 clocks | 3'h7 | 7 clocks |

Note: DIVI (R90h) sets division ratio of clock frequency.

Panel Interface Control 4 (R94h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|----------|----------|----------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SDT I[2] | SDT I[1] | SDT I[0] |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

SDTI[2:0]: Defines source output alternating position within 1H period.

SDTI is disabled when RGB interface is selected.

Table 51

| SDTI[2:0] | Source output alternating position |
|------------------|---|
| 3'h0 | Setting inhibited |
| 3'h1 | 1 clock |
| 3'h2 | 2 clocks |
| 3'h3 | 3 clocks |
| 3'h4 | 4 clocks |
| 3'h5 | 5 clocks |
| 3'h6 | 6 clocks |
| 3'h7 | 7 clocks |

Note: DIVI (R90h) sets division ratio of clock frequency.

Panel Interface Control 5 (R95h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------|-------------|-------------|-----|-----|-------------|-------------|-------------|-------------|-------------|-------------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | DIVE [1] | DIVE [0] | 0 | 0 | RTN E[5] | RTN E[4] | RTN E[3] | RTN E[2] | RTN E[1] | RTN E[0] |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

RTNE[5:0]: Sets RTNE[5:0] and DIVE[1:0] bits so that the number of DOTCLK calculated from the following formula becomes the number of DOTCLK which should be inputted in 1H period. The RTNE[5:0] setting is enabled in display operation via RGB interface.

$(PCDIVH + PCDIVL) \times DIVE[1:0]$ (division ratio) \times RTNE[5:0] (Number of DOTCLK) \leq Number of DOTCLK in 1H period

DIVE[1:0]: Sets the division ratio of DOTCLK frequency. The R61505W's internal operation is synchronized with the frequency divided DOTCLK. The setting in DIVE[1:0] is enabled in RGB interface operation.

Table 52 Division Ratio of DOTCLK

| DIVE[1:0] | Division Ratio |
|-----------|------------------|
| 2'h0 | Setting disabled |
| 2'h1 | 1/4 |
| 2'h2 | 1/8 |
| 2'h3 | 1/16 |

Internal clock frequency is calculated by below formula:

$$\text{DOTCLK} / (\text{DIVE} \times (\text{PCDIVL} + \text{PCDIVH}))$$

See also R9Ch.

Table 53 DOTCLK per Line (1H Period)

| RTNE[5:0] | DOTCLK per line (1H) | RTNE[5:0] | DOTCLK per line (1H) |
|------------------|-----------------------------|------------------|-----------------------------|
| 6'h00 | Setting disabled | 6'h20 | 32 clocks |
| 6'h01 | Setting disabled | 6'h21 | 33 clocks |
| 6'h02 | Setting disabled | 6'h22 | 34 clocks |
| 6'h03 | Setting disabled | 6'h23 | 35 clocks |
| 6'h04 | Setting disabled | 6'h24 | 36 clocks |
| 6'h05 | Setting disabled | 6'h25 | 37 clocks |
| 6'h06 | Setting disabled | 6'h26 | 38 clocks |
| 6'h07 | Setting disabled | 6'h27 | 39 clocks |
| 6'h08 | Setting disabled | 6'h28 | 40 clocks |
| 6'h09 | Setting disabled | 6'h29 | 41 clocks |
| 6'h0A | Setting disabled | 6'h2A | 42 clocks |
| 6'h0B | Setting disabled | 6'h2B | 43 clocks |
| 6'h0C | Setting disabled | 6'h2C | 44 clocks |
| 6'h0D | Setting disabled | 6'h2D | 45 clocks |
| 6'h0E | Setting disabled | 6'h2E | 46 clocks |
| 6'h0F | Setting disabled | 6'h2F | 47 clocks |
| 6'h10 | 16 clocks | 6'h30 | 48 clocks |
| 6'h11 | 17 clocks | 6'h31 | 49 clocks |
| 6'h12 | 18 clocks | 6'h32 | 50 clocks |
| 6'h13 | 19 clocks | 6'h33 | 51 clocks |
| 6'h14 | 20 clocks | 6'h34 | 52 clocks |
| 6'h15 | 21 clocks | 6'h35 | 53 clocks |
| 6'h16 | 22 clocks | 6'h36 | 54 clocks |
| 6'h17 | 23 clocks | 6'h37 | 55 clocks |
| 6'h18 | 24 clocks | 6'h38 | 56 clocks |
| 6'h19 | 25 clocks | 6'h39 | 57 clocks |
| 6'h1A | 26 clocks | 6'h3A | 58 clocks |
| 6'h1B | 27 clocks | 6'h3B | 59 clocks |
| 6'h1C | 28 clocks | 6'h3C | 60 clocks |
| 6'h1D | 29 clocks | 6'h3D | 61 clocks |
| 6'h1E | 30 clocks | 6'h3E | 62 clocks |
| 6'h1F | 31 clocks | 6'h3F | 63 clocks |

Panel Interface Control 5-1 (R96h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|------------------|------------------|------------------|------------------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SPC WE [3] | SPC WE [2] | SPC WE [1] | SPC WE [0] |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

SPCWE [3:0]: The bit is used to set source VCI pre-charge period. Pre-charge period is set by SPCWE[3:0] starting from the source output alternating position defined by SDTE[2:0]. This bit is enabled when RGB interface is selected.

Table 54

| SPCWE [3:0] | Source VCI pre-charge period |
|------------------------|-------------------------------------|
| 4'h0 | 0 clocks |
| 4'h1 | 1 clock |
| 4'h2 | 2 clocks |
| 4'h3 | 3 clocks |
| 4'h4 | 4 clocks |
| 4'h5 | 5 clocks |
| 4'h6 | 6 clocks |
| 4'h7 | 7 clocks |
| 4'h8 | 8 clocks |
| 4'h9 | 9 clocks |
| 4'hA | 10 clocks |
| 4'hB | 11 clocks |
| 4'hC | 12 clocks |
| 4'hD | 13 clocks |
| 4'hE | 14 clocks |
| 4'hF | 15 clocks |

Panel Interface Control 6 (R97h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|-------------|-------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | 0 | 0 | NOW E[2] | NOW E[1] | NOW E[0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

NOWE[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

Table 55**NOWE [2:0] Non-overlap period**

| | |
|------|------------------|
| 3'h0 | Setting disabled |
| 3'h1 | 1 |
| 3'h2 | 2 |
| 3'h3 | 3 |
| 3'h4 | 4 |
| 3'h5 | 5 |
| 3'h6 | 6 |
| 3'h7 | 7 |

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH) [DOTCLK].

Panel Interface Control 7 (R98h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|-----------|-----------|-----------|-----|-----|-----|-----|-----|----------|----------|----------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | VEQWE [2] | VEQWE [1] | VEQWE [0] | 0 | 0 | 0 | 0 | 0 | MCPE [2] | MCPE [1] | MCPE [0] |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

VEQWE [2:0]: VEQWE sets VCOM equalize period. Equalizing operation continues for the period defined by VEQWE bit starting from the VCOM alternating position defined by MCPE [2:0]. VEQWE setting is enabled when VEM[1:0]=1 or larger (R0Eh).

Table 56**VEQWE[2:0] VCOM equalize period**

| | |
|------|----------|
| 3'h0 | 0 clocks |
| 3'h1 | 1 clock |
| 3'h2 | 2 clocks |
| 3'h3 | 3 clocks |
| 3'h4 | 4 clocks |
| 3'h5 | 5 clocks |
| 3'h6 | 6 clocks |
| 3'h7 | 7 clocks |

MCPE[2:0]: Sets the source output timing by the number of internal clock from the reference point. The setting is enabled in display operation via RGB interface.

Table 57

| MCPE[2:0] | Source output position | MCPE[2:0] | Source output position |
|-----------|------------------------|-----------|------------------------|
| 3'h0 | Setting Disabled | 3'h4 | 4 clocks |
| 3'h1 | 1 clock | 3'h5 | 5 clocks |
| 3'h2 | 2 clocks | 3'h6 | 6 clocks |
| 3'h3 | 3 clocks | 3'h7 | 7 clocks |

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH) [DOTCLK].

Panel Interface Control 8 (R99h)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Default value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

SDTE[2:0]: Defines source output alternating position within 1H period.

SDTE is enabled when RGB interface is selected.

Table 58

| SDTE[2:0] | Source output alternating position |
|------------------|---|
| 3'h0 | Setting inhibited |
| 3'h1 | 1 clock |
| 3'h2 | 2 clocks |
| 3'h3 | 3 clocks |
| 3'h4 | 4 clocks |
| 3'h5 | 5 clocks |
| 3'h6 | 6 clocks |
| 3'h7 | 7 clocks |

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH) [DOTCLK]

Panel Interface Control 9 (R9Ch)

| R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------|----|------|------|------|------|------|------|-----|-----|-----|---------------|---------------|---------------|-----|---------------|---------------|---------------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PCDIVH [2] | PCDIVH [1] | PCDIVH [0] | 0 | PCDIVL [2] | PCDIVL [1] | PCDIVL [0] |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |

PCDIVH[2:0], PCDIVL[2:0]:

When DM [1:0] = 2'h1 and RGB I/F is selected, internal clock used for display operation switches from internal oscillation to DOTCLKD. PCDIVH and PCDIVL bits define division ratio of DOTCLKD to DOTCLK.

PCDIVH defines number of DOTCLK during DOTCLKD is high in the units of 1 clock.

PCDIVL defines number of DOTCLK during DOTCLKD is low in the units of 1 clock.

Make sure that PCDIVL = PCDIVH or PCDIVH-1.

Also, write PCDIVH and PCDIVL values so that DOTCLKD frequency is the closest to internal oscillation clock frequency 600 KHz.

See “Setting Example of Display Control Clock in RGB Interface Operation” for details.

Table 59

| PCDIVH[2:0] | |
|--------------------|-------------------|
| 3'h0 | Setting inhibited |
| 3'h1 | 1 clock |
| 3'h2 | 2 clocks |
| 3'h3 | 3 clocks |
| 3'h4 | 4 clocks |
| 3'h5 | 5 clocks |
| 3'h6 | 6 clocks |
| 3'h7 | 7 clocks |

Table 60

| PCDIVL[2:0] | |
|--------------------|-------------------|
| 3'h0 | Setting inhibited |
| 3'h1 | 1 clock |
| 3'h2 | 2 clocks |
| 3'h3 | 3 clocks |
| 3'h4 | 4 clocks |
| 3'h5 | 5 clocks |
| 3'h6 | 6 clocks |
| 3'h7 | 7 clocks |

NVM Control

NVM Control 1 (RA0h), NVM Control 2 (RA1h)

| | R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------|---------|----|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| R A0 | R/W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TE | 0 | EOP [1] | EOP [0] | 0 | 0 | 0 | NV AD |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R A1 | R/W | 1 | NV DAT [15] | NV DAT [14] | NV DAT [13] | NV DAT [12] | NV DAT [11] | NV DAT [10] | NV DAT [9] | NV DAT [8] | NV DAT [7] | NV DAT [6] | NV DAT [5] | NV DAT [4] | NV DAT [3] | NV DAT [2] | NV DAT [1] | NV DAT [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TE: Enables access to the NVM when TE=1.

EOP [1:0]: Internal NVM control bits to control write and erase operations.

Table 61

| EOP[1:0] | NVM control |
|----------|------------------|
| 2'h0 | Halt |
| 2'h1 | Write |
| 2'h2 | Setting disabled |
| 2'h3 | Erase |

NVAD: Specifies address to access on the NVM for write and erase operation. An address consists of 16 bits. To write to the NVM, write the data that users wish to write in NVDAT (RA1h) and write EOP=2'h1 to enable the write operation. To erase, define the address users wish to erase data from and write EOP=2'h3 to enable the erase operation. See “NVM Control Sequence” for details.

Table 62

| NVAD | NVDAT [15]/[7] | NVDAT [14]/[6] | NVDAT [13]/[5] | NVDAT [12]/[4] | NVDAT [11]/[3] | NVDAT [10]/[2] | NVDAT [9]/[1] | NVDAT [8]/[0] |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------------------|------------------|
| 1'h0 (MS byte) | VCMSEL | VCM2 [6] | VCM2 [5] | VCM2 [4] | VCM2 [3] | VCM2 [2] | VCM2 [1] | VCM2 [0] |
| 1'h0 (LS byte) | 1 | VCM1 [6] | VCM1 [5] | VCM1 [4] | VCM1 [3] | VCM1 [2] | VCM1 [1] | VCM1 [0] |
| 1'h1 (MS byte) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1'h1 (LS byte) | UID1 [7] | UID1 [6] | UID1 [5] | UID1 [4] | UID1 [3] | UID1 [2] | UID1 [1] | UID1 [0] |

MS byte =NVDAT [15:8]. LS byte=NVDAT [7:0].

VCM1[6:0]: Defines factor to adjust VCOMH level when VCMSEL=1.

VCM2[6:0]: Defines factor to adjust VCOMH level when VCMSEL=0.

UID1[7:0]: User ID.

NVM Control 3 (RA3h)

| | R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------|---------|----|------|------|------|------|------|------|-----|-----|-----|-----|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| R A3 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VER IFL GER | VER IFL GWR | RTY RTL [3] | RTY RTL [2] | RTY RTL [1] | RTY RTL [0] |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VERIFLGER: Before data is written to NVM, a verify operation is automatically performed by erasing data from the specified address. For details, see “NVM Write Sequence” in “NVM Control Sequence”. If the verify operation after the erase operation passes, VERIFLGER is set to “1”. If it fails, VERIFLGER remains “0”.

VERIFLGWR: After data has been written to NVM, a verify operation is automatically performed. For details, see “NVM Write Sequence” and “NVM Erase Sequence” in “NVM Control Sequence”. If the verify operation after the write operation passes, VERIFLGWR is set to “1”. If it fails, VERIFLGWR remains “0”.

RTYRTL[3:0]: After data has been written to NVM, the number of times data is verified during the internal sequence is read. For details, see “NVM Write Sequence” and “NVM Erase Sequence”.

NVM Control 4 (RA4h)

| | R/W | RS | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---------|---------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| R A4 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CAL B |
| | Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

CALB: When CALB=1, all data in NVM is read out and written to internal registers. When finished, CALB is set to 0.

Reset Function

The R61505W is initialized by the RESET input. During reset period, the R61505W is in a busy state and instruction from the host processor and frame memory access are not accepted. The R61505W's internal power supply circuit unit is initialized also by the RESET input.

1. Initial state of instruction bits (default)

See the instruction list. The default values are shown in the parenthesis of each instruction bit cell.

2. Frame memory data initialization

The frame memory data is not automatically initialized by the RESET input. It must be initialized by software in display-off period.

3. Output pin initial state

| Pin name | After H/W reset |
|-----------|-----------------|
| DB[17:0] | Hi-Z |
| SDO | Hi-Z |
| FMARK | GND |
| VDD | 1.5V |
| VCI1 | Hi-Z |
| C11P/C11M | Hi-Z/Hi-Z |
| C12P/C12M | Hi-Z/Hi-Z |
| C13P/C13M | Hi-Z/GND |
| C21P/C21M | VCI/GND |
| C22P/C22M | VCI/GND |
| VREG1OUT | GND |
| VCOML | GND |
| VCOMH | VCI(DDVDH) |
| VCL | GND |
| VGL | GND |
| VGH | VCI |
| DDVDH | VCI |
| VCOM | GND |
| S[720:1] | GND |
| G[320:1] | GND |

Basic Operation

The basic operation modes of the R61505W are shown in the following diagram. When making a transition from one mode to another, refer to instruction setting sequence.

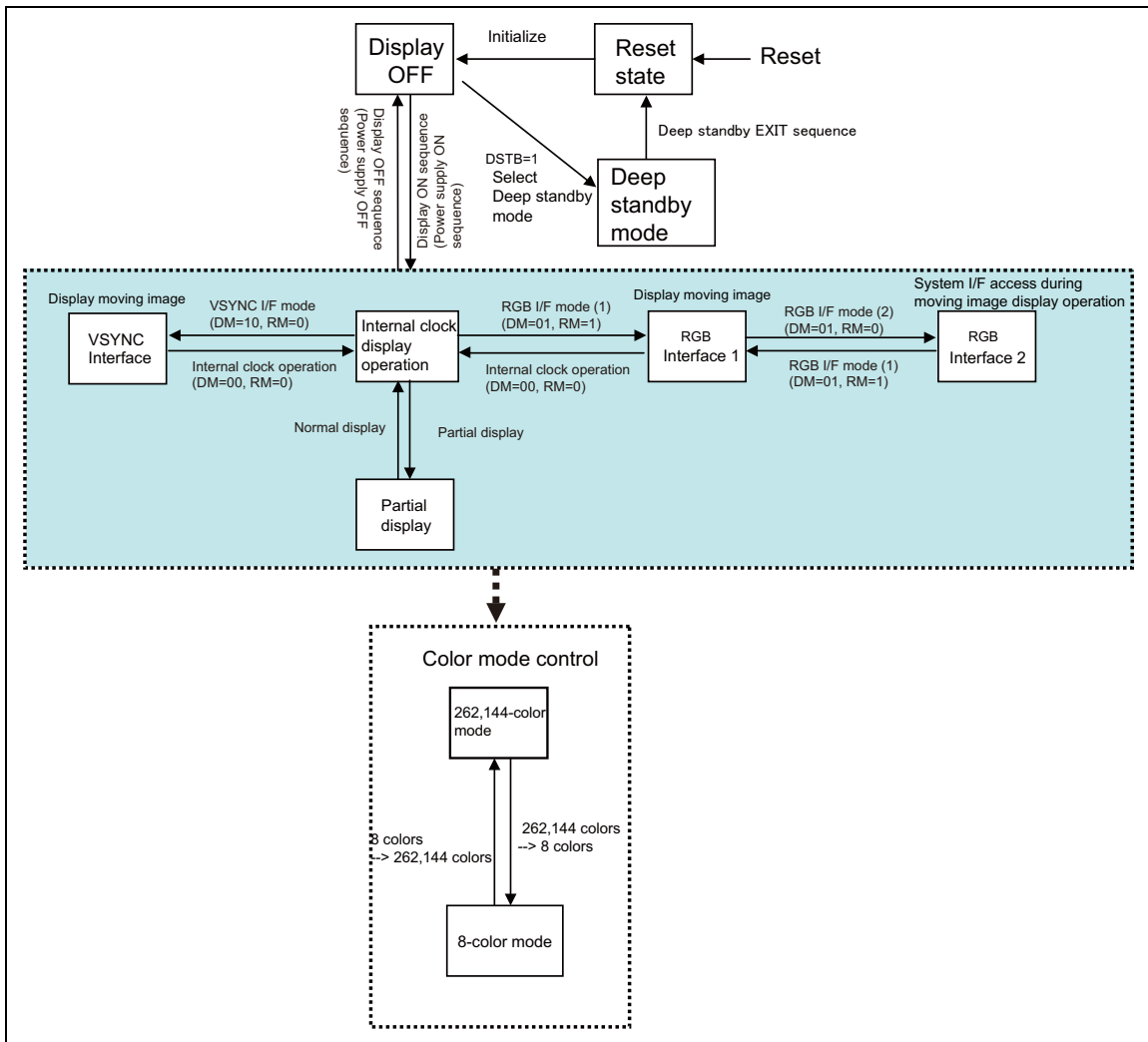


Figure 10

Interface and Data Format

The R61505W supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The R61505W can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the R61505W supports RGB interface and VSYNC interface, which enables data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the R61505W writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB[17:0]). The display data is stored in the R61505W's frame memory so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the frame memory area to write data for moving picture display, which enables displaying a moving picture and frame memory data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the frame memory at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal frame memory.

The R61505W operates in either one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register (R0Ch). When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Table 63 Operation Modes

| Operation Mode | Frame memory Access Setting (RM) | Display Operation Mode (DM) |
|---|----------------------------------|---------------------------------------|
| Internal clock operation (displaying still pictures) | System interface (RM = 0) | Internal clock operation (DM1-0 = 00) |
| RGB interface (1) (displaying moving pictures) | RGB interface (RM = 1) | RGB interface (DM1-0 = 01) |
| RGB interface (2) (rewriting still pictures while displaying moving pictures) | System interface (RM = 0) | RGB interface (DM1-0 = 01) |
| VSYNC interface (displaying moving pictures) | System interface (RM = 0) | VSYNC interface (DM1-0 = 10) |

- Notes:
1. Instructions are set only via system interface.
 2. The RGB and VSYNC interfaces cannot be used simultaneously.
 3. Do not change RGB interface operation setting (RIM1-0) during RGB interface operation.
 4. See the "External Display Interface" section for the sequences when switching from one mode to another.

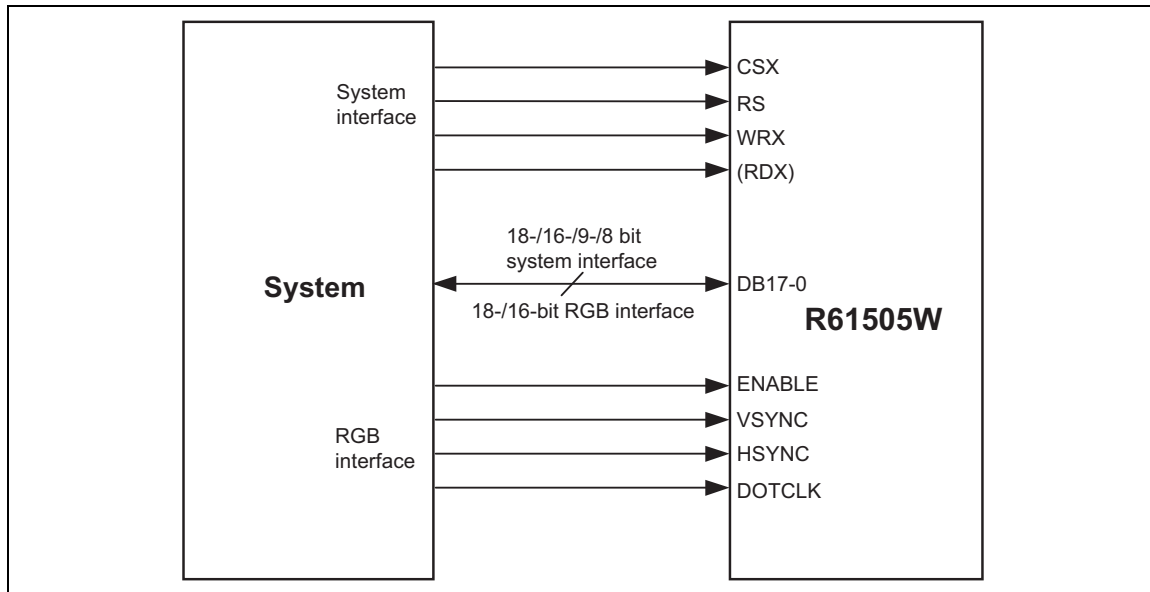


Figure 11

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal frame memory can be accessed only via system interface.

RGB interface operation (1)

The display operation is synchronized with frame synchronous signal (VSYNC), line synchronous signal (HSYNC), and dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied during the display operation via RGB interface.

The R61505W transfers display data in units of pixels via DB[17:0] pins. The display data is stored in the internal frame memory. Window address function can minimize the total number of data transfer for moving picture display because only the moving picture data is transferred to the frame memory, enabling the R61505W to display a moving picture and another image stored in the frame memory simultaneously.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the R61505W by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB[17:0] pins in accordance with the setting of these periods.

RGB interface operation (2)

This mode enables the R61505W to rewrite frame memory data via system interface while using RGB interface for display operation. To rewrite frame memory data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first. Then set an address in the frame memory address set register and R22h in the index register.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the R61505W to display a moving picture via system interface by writing data in the internal frame memory at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing frame memory data. For details, see the “VSYNC Interface” section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the R61505W according to the instruction settings for these periods.

FMARK interface operation

In the FMARK interface operation, data is written to internal frame memory via system interface synchronizing with the frame mark signal (FMARK), realizing tearing-less moving picture while using conventional system interface. In this case, there are restrictions in speed and method of writing frame memory data. See “FMARK Interface” for details.

System Interface

The following are the kinds of system interfaces available with the R61505W. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and frame memory access.

Table 64 IM Bit Settings and System Interface

| IM3 | IM2 | IM1 | IM0 | Interfacing Mode with Host processor | DB Pins | Colors |
|-----|-----|-----|-----|--------------------------------------|-----------------------|-----------------------|
| 0 | 0 | 0 | 0 | Setting inhibited | - | - |
| 0 | 0 | 0 | 1 | Setting inhibited | - | - |
| 0 | 0 | 1 | 0 | 80-system 16-bit interface | DB[17:10], DB[8:1] | 262,144 *see Note1 |
| 0 | 0 | 1 | 1 | 80-system 8-bit interface | DB[17:10] | 262,144 *see Note2 |
| 0 | 1 | 0 | 0 | Clock synchronous serial interface | - | 65,536 |
| 0 | 1 | 1 | 0 | Setting inhibited | - | - |
| 0 | 1 | 1 | 1 | Setting inhibited | - | - |
| 1 | 0 | 0 | 0 | Setting inhibited | - | - |
| 1 | 0 | 0 | 1 | Setting inhibited | - | - |
| 1 | 0 | 1 | 0 | 80-system 18-bit interface | DB[17:0] | 262,144 |
| 1 | 0 | 1 | 1 | 80-system 9-bit interface | DB[17:9] | 262,144 |
| 1 | 1 | 0 | 0 | Setting inhibited | - | - |
| 1 | 1 | 0 | 1 | Setting inhibited | - | - |
| 1 | 1 | 1 | 0 | Setting inhibited | - | - |
| 1 | 1 | 1 | 1 | Setting inhibited | - | - |

Notes: 1. 262,144 colors in 16-bit 2-transfer mode. 65,536 colors in 16-bit 1-transfer mode.
2. 262,144 colors in 8-bit 3-transfer mode. 65,536 colors in 8-bit 2-transfer mode.

80-System 18-Bit Bus Interface

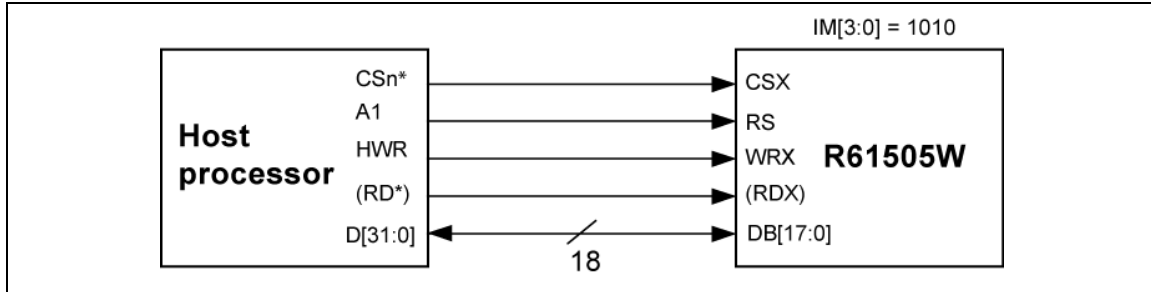


Figure 12 18-Bit Interface

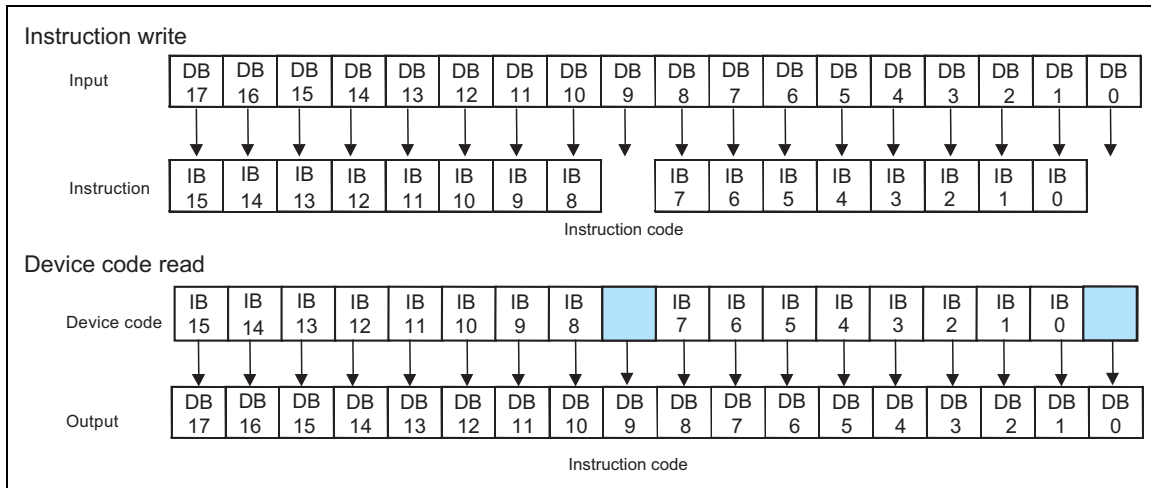


Figure 13 18-Bit Interface Data Format (Instruction Write / Device Code Read) (IM[3:0]=1010)

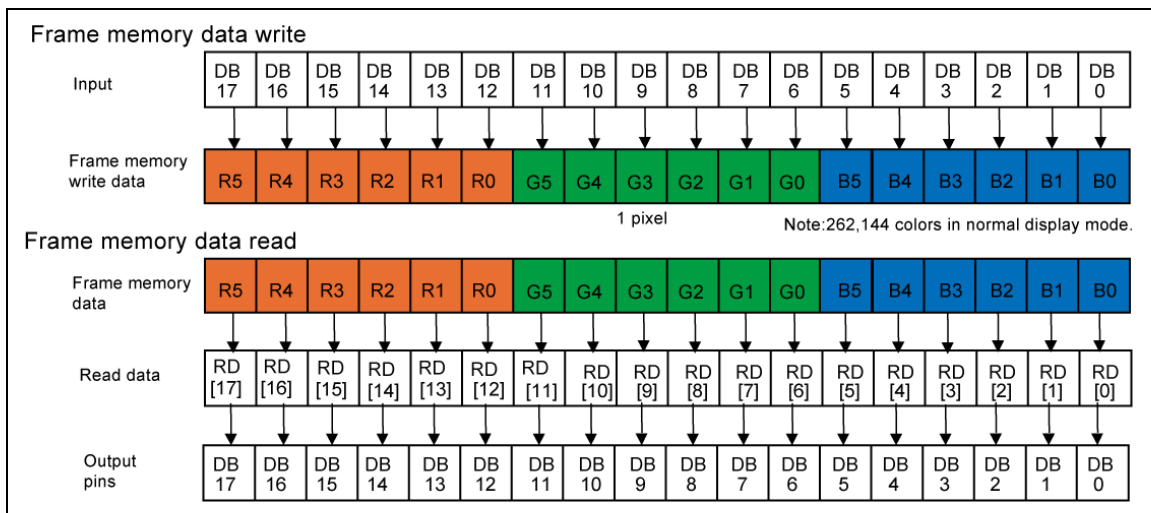


Figure 14 18-Bit Interface Data Format (Frame Memory Data Write / Frame Memory Data Read)

80-System 16-Bit Bus Interface

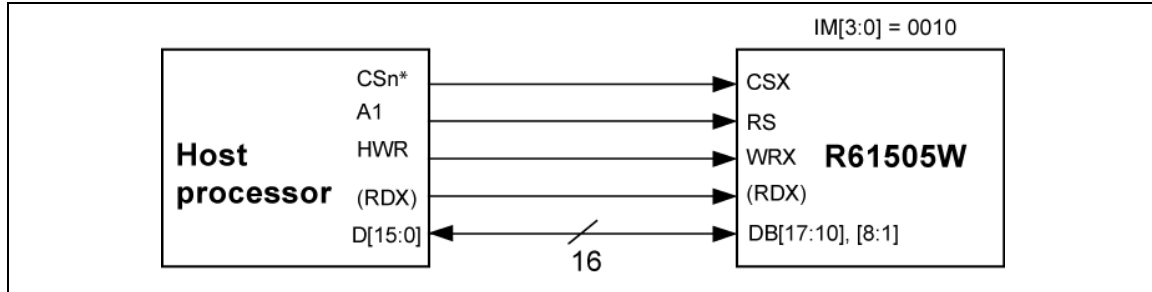


Figure 15 16-Bit Interface

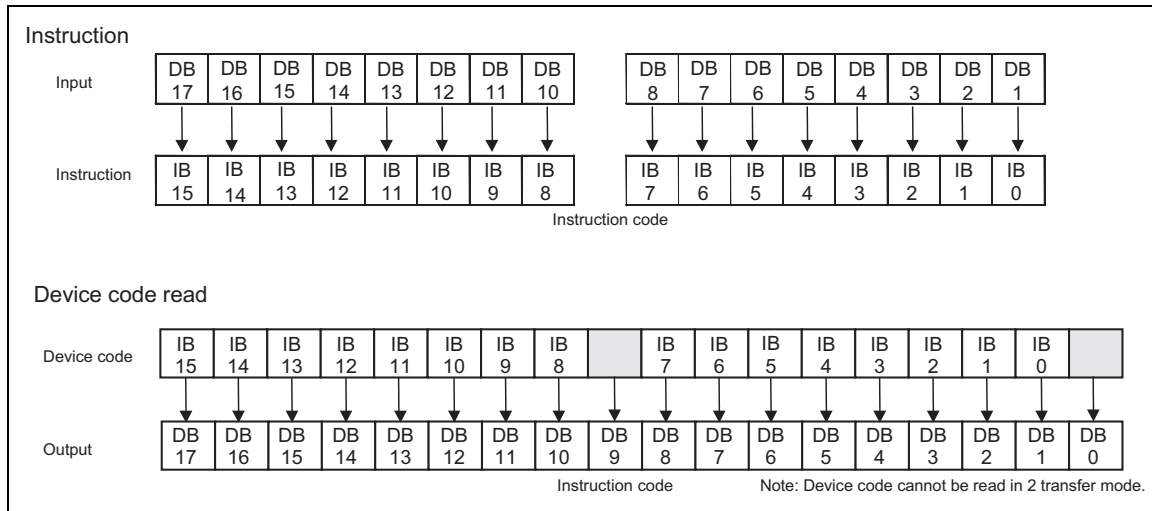


Figure 16 16-Bit Interface Data Format (Instruction Write / Device Code Read)

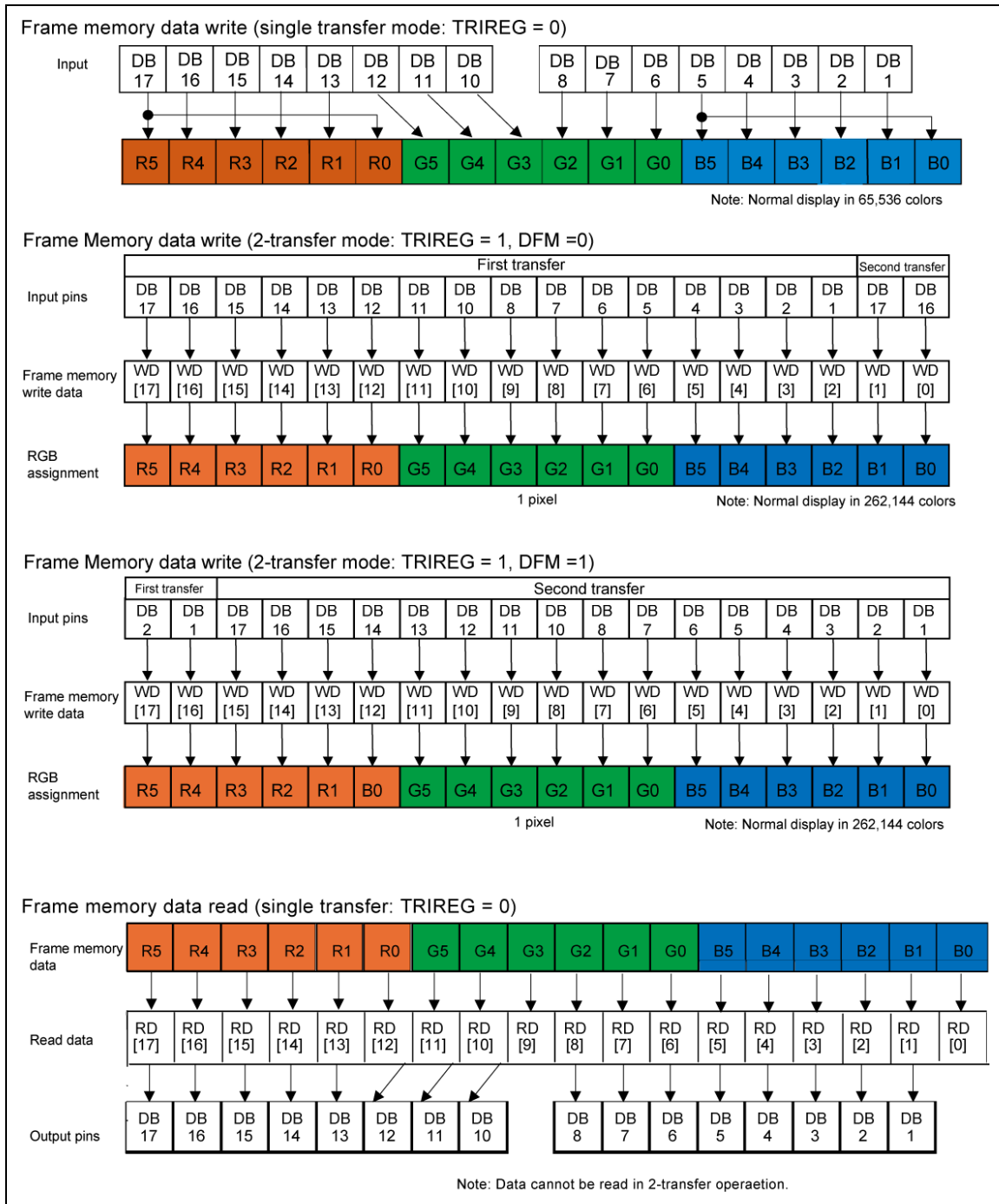


Figure 17 16-Bit Interface Data Format (Frame Memory Data Write / Frame Memory Data Read)

Data Transfer Synchronization in 16-Bit Bus Interface Operation

The R61505W supports data transfer synchronization function to reset the counters for upper 16-/2-bit and lower 2-/16-bit transfers in 16-bit 2-transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 2/16 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

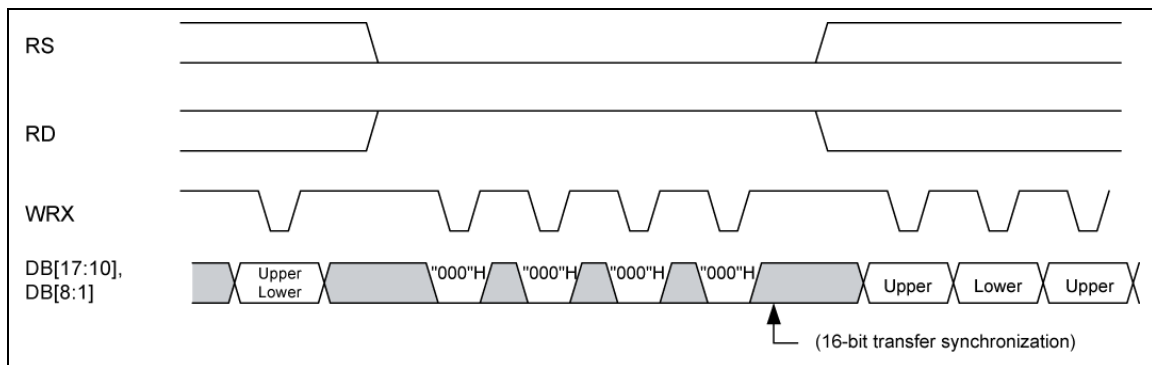


Figure 18 16-Bit Data Transfer Synchronization

80-System 9-Bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The frame memory write data is also divided into upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either IOVCC or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

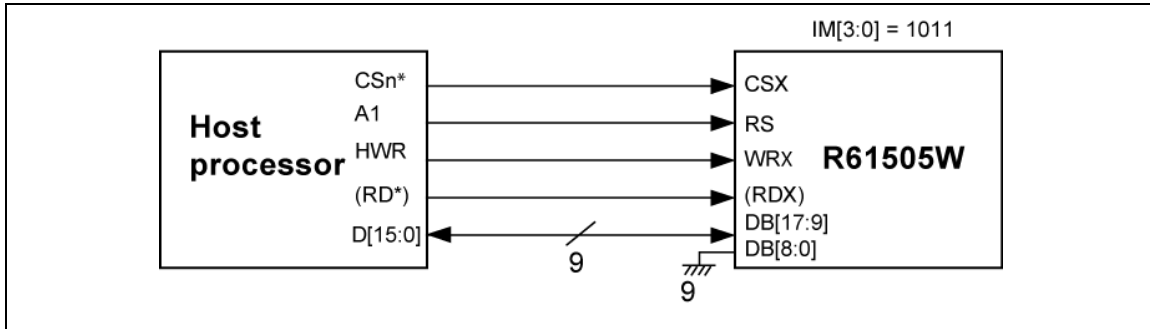


Figure 19 9-Bit Interface

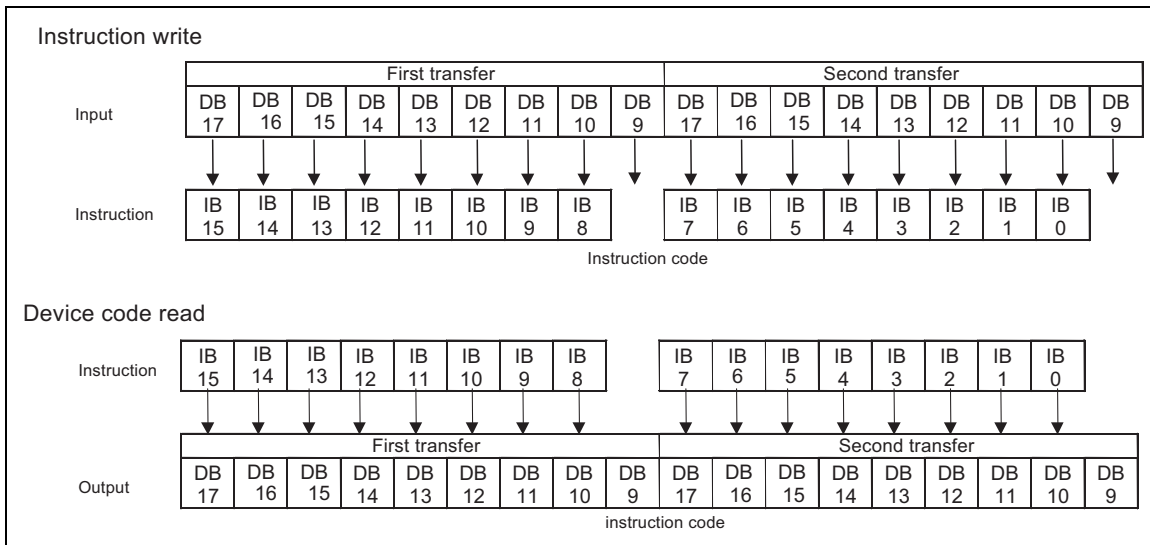


Figure 20 9-Bit Interface Data Format (Instruction Write / Device Code Read)

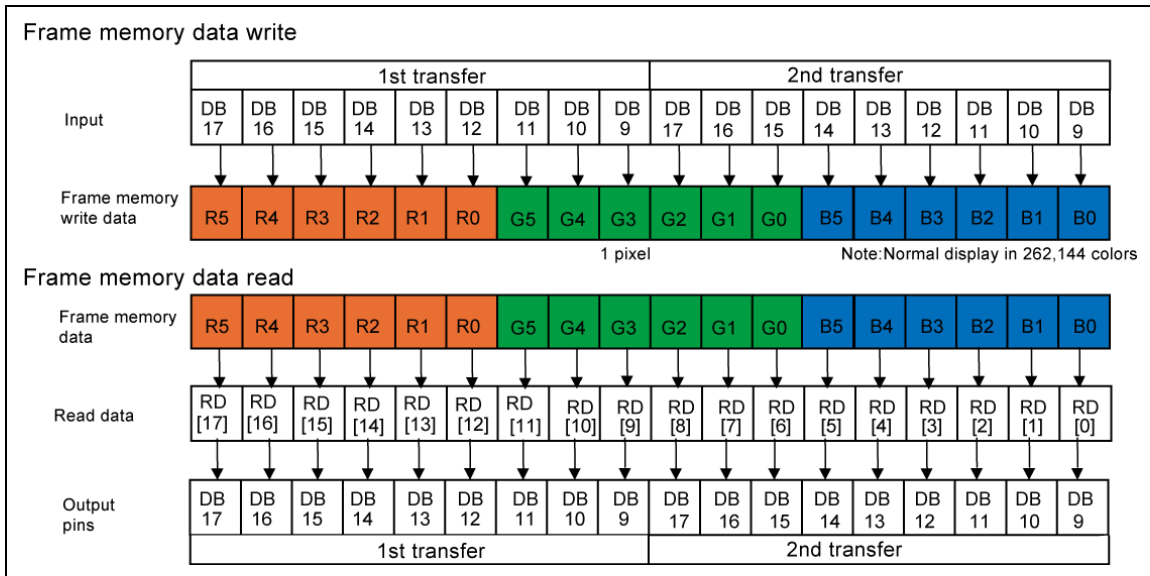


Figure 21 9-Bit Interface Data Format (Frame Memory Data Write/ Frame Memory Data Read)

Data Transfer Synchronization in 9-Bit Bus Interface Operation

The R61505W supports data transfer synchronization function to reset the counters for upper and lower 9-bit transfers in 9-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 9 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

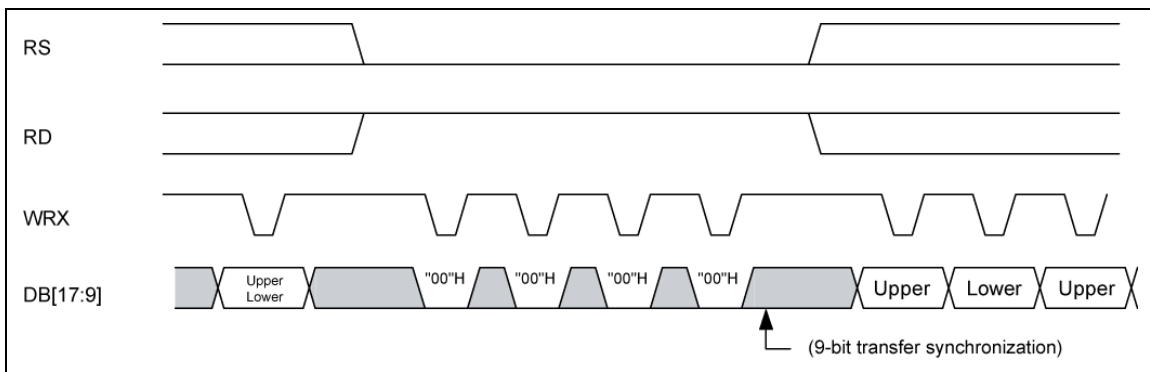


Figure 22 9-Bit Data Transfer Synchronization

80-System 8-Bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The frame memory write data is also divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The frame memory write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either IOVCC or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

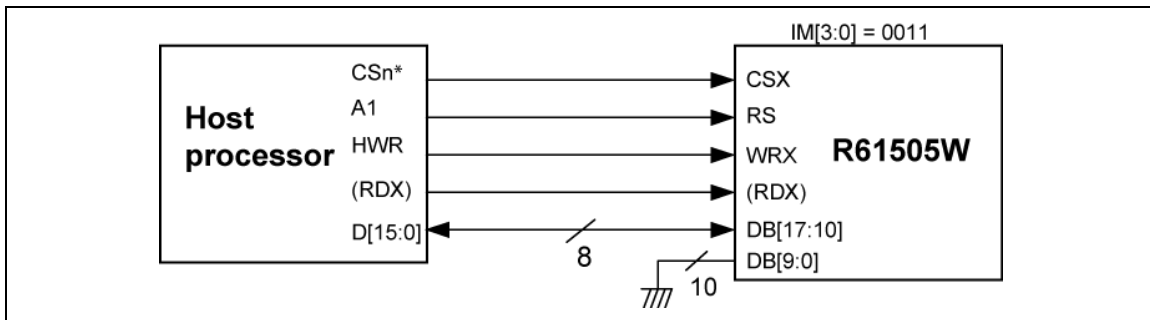


Figure 23 8-Bit Interface

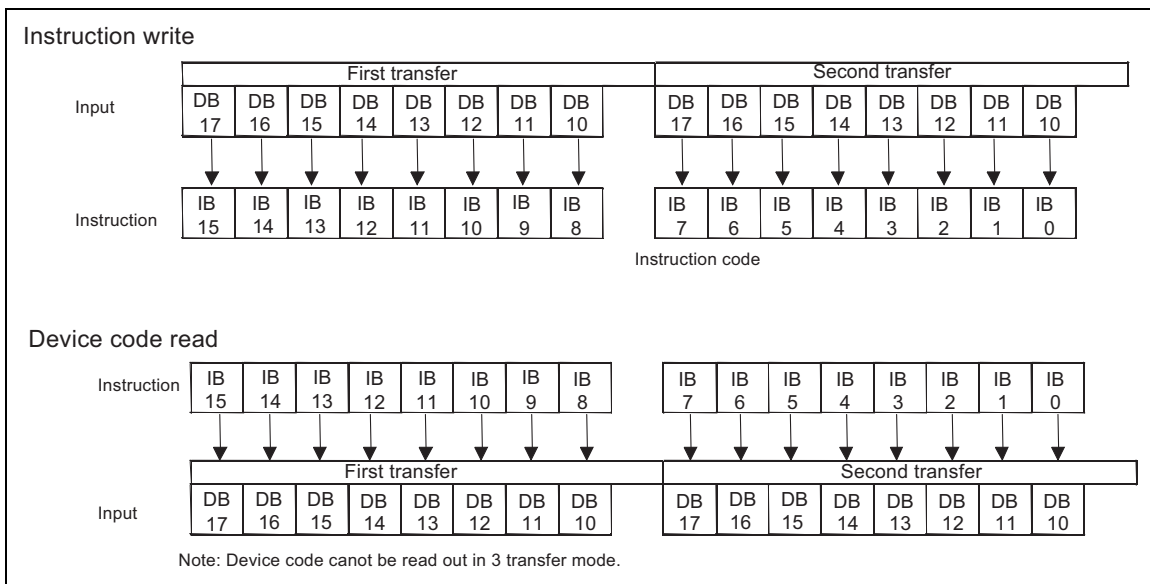


Figure 24 8-Bit Interface Data Format (Instruction Write / Device Code Read)

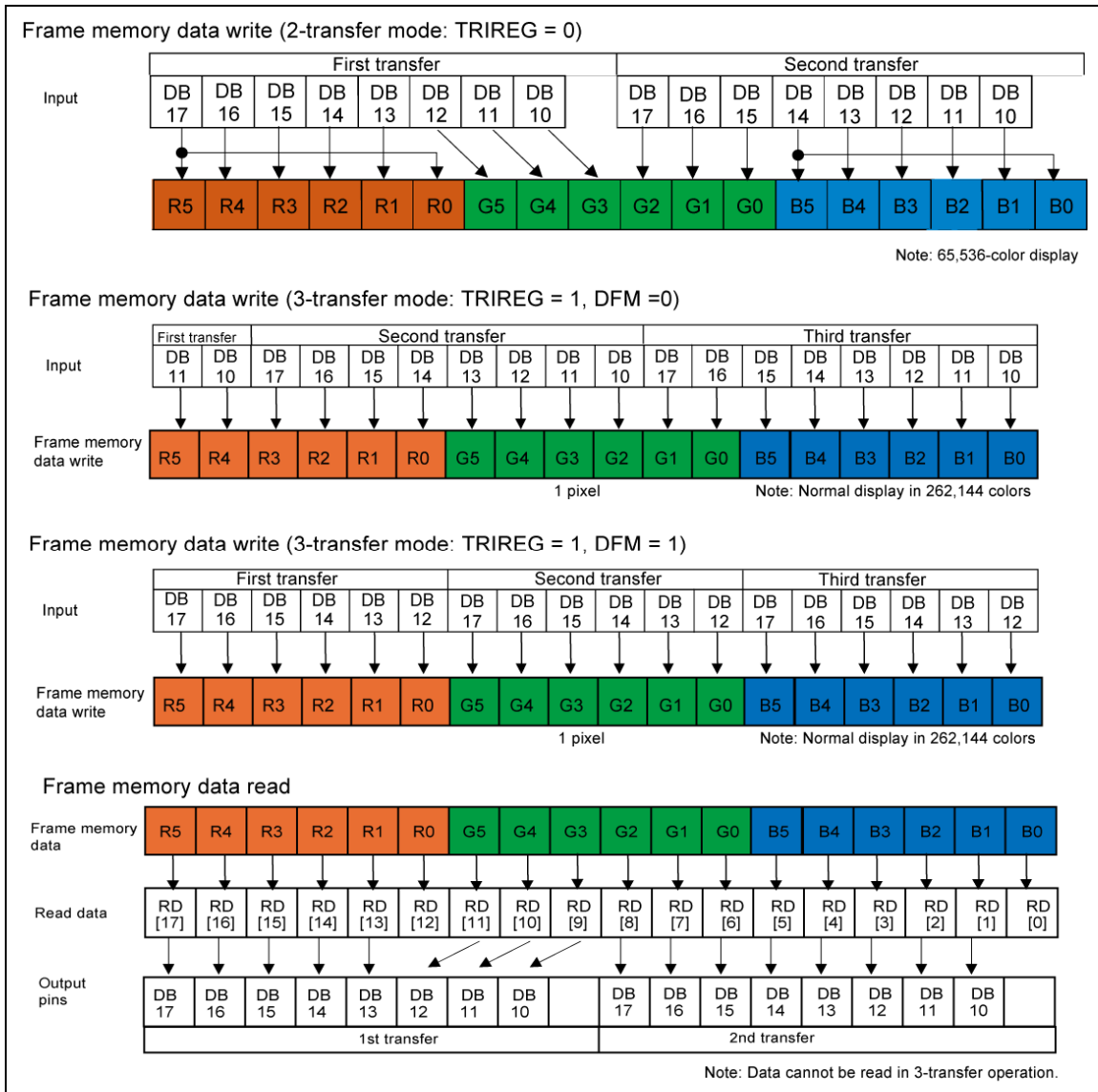


Figure 25 8-Bit Interface Data Format (Frame Memory Data Write / Frame Memory Data Read)

Data Transfer Synchronization in 8-Bit Bus Interface operation

The R61505W supports data transfer synchronization function to reset the counters for upper and lower 8-bit transfers in 8-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 8 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

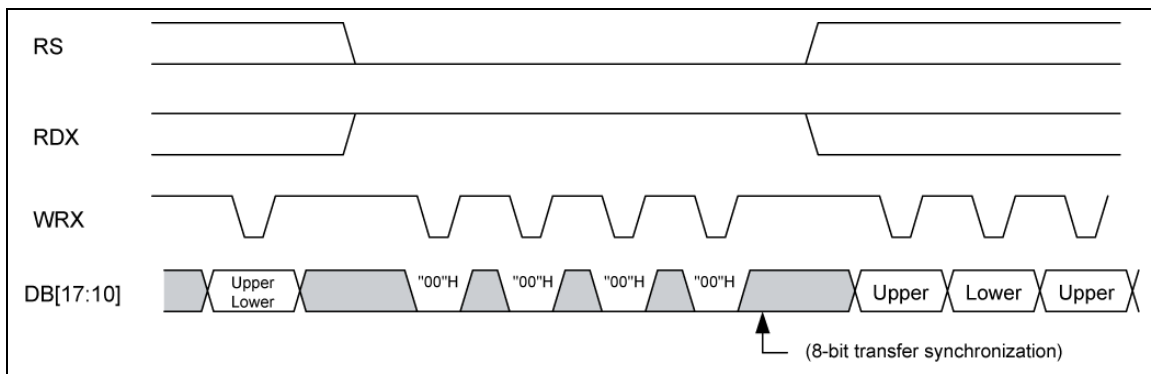


Figure 26 8-Bit Data Transfer Synchronization

Serial Interface

The serial interface is selected by setting the IM3/2/1/0 pins to the GND/IOVCC/GND/GND levels, respectively. The data is transferred via chip select line (CSX), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, unused DB[17:0] pins must be fixed at either IOVCC or GND level.

The R61505W recognizes the start of data transfer on the falling edge of CSX input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CSX input. The R61505W is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code (“011100”) assigned to the R61505W are compared and agreed. Then, the R61505W starts taking in subsequent data. Two different chip addresses must be assigned to the R61505W because the seventh bit of the start byte is register select bit (RS). When RS = 0, index register write operation is executed. When RS = 1, either instruction write operation or frame memory read/write operation is executed. The eighth bit of the start byte is R/W bit, which selects either read or write operation. The R61505W receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the frame memory via serial interface, the data is written to the frame memory after it is transferred in two bytes. The R61505W writes data to the frame memory in units of 18 bits by adding the same bits as the MSBs to the LSBs of R dot data and B dot data.

After receiving the start byte, the R61505W starts transferring or receiving data in units of bytes. The R61505W transfers data from the MSB. The R61505W’s instruction consists of 16 bits and it is executed inside the R61505W after it is transferred in two bytes (16 bits: DB[15:0]) from the MSB. The R61505W expands frame memory write data into 18 bits when writing them to the internal frame memory. The first byte received by the R61505W following the start byte is recognized as the upper eight bits of instruction and the second byte is recognized as the lower 8 bits of instruction.

When reading data from the frame memory, valid data is not transferred to the data bus until first five bytes of data are read from the frame memory following the start byte. The R61505W sends valid data to the data bus when it reads the sixth and subsequent byte data.

Table 65 Start Byte Format

| Transferred Bits | S | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|-------------------|----------------|----------------|---|---|---|---|---|----|-----|
| Start byte format | Transfer start | Device ID code | | | | | | RS | R/W |
| | | 0 | 1 | 1 | 1 | 0 | 0 | | |

Table 66 Functions of RS, R/W Bits

| RS | R/W | Function |
|----|-----|---|
| 0 | 0 | Set index register |
| 0 | 1 | Setting inhibited |
| 1 | 0 | Write instruction or frame memory data |
| 1 | 1 | Read register settings or frame memory data |

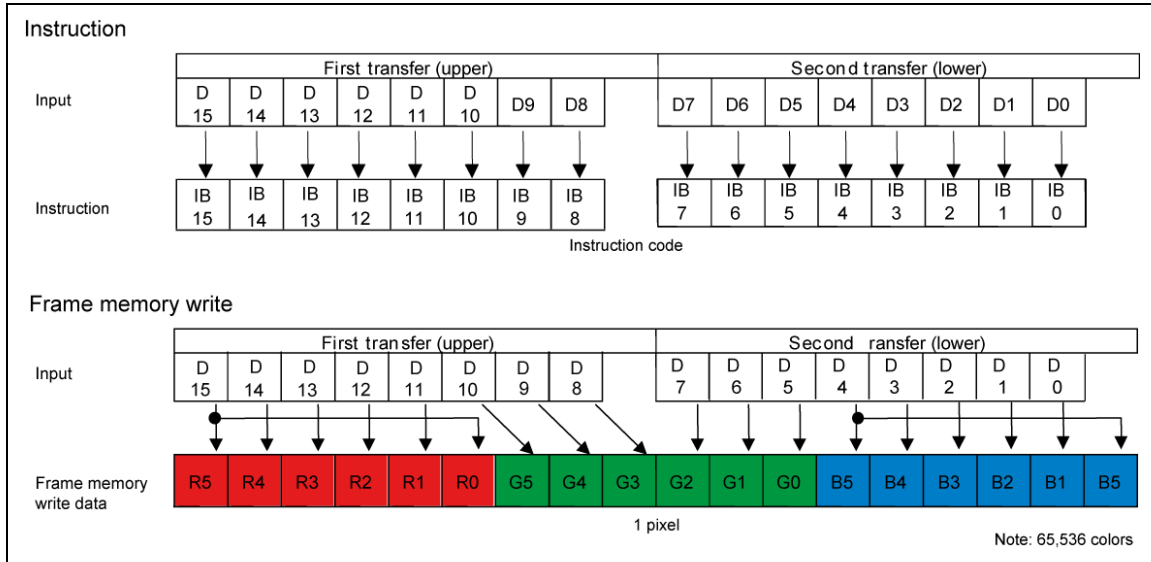
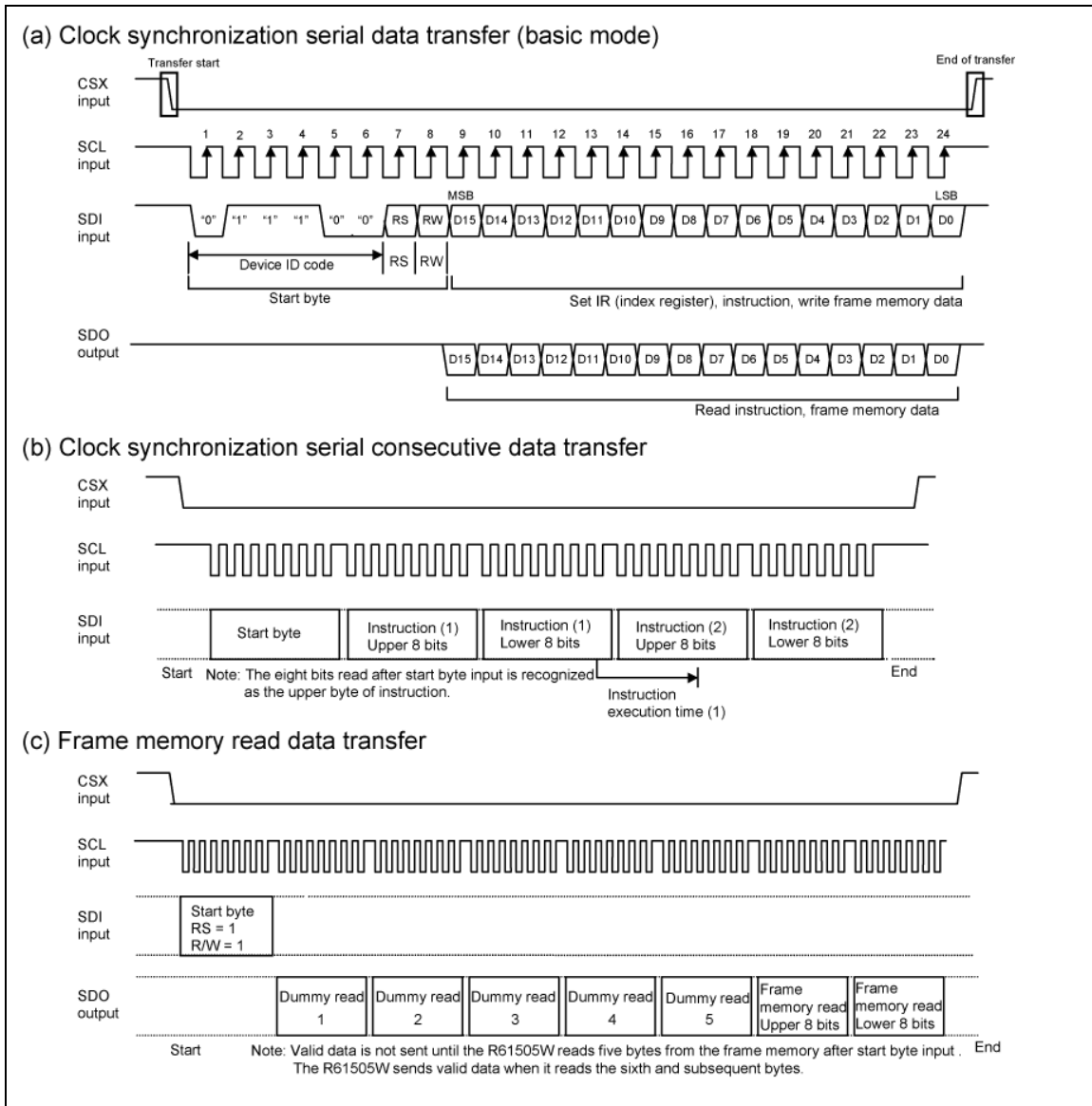


Figure 27 Serial Interface Data Format



VSYNC Interface

The R61505W supports VSYNC interface, which enables displaying a moving picture via system interface by synchronizing the display operation with the VSYNC signal. VSYNC interface can realize moving picture display with minimum modification to the conventional system operation.

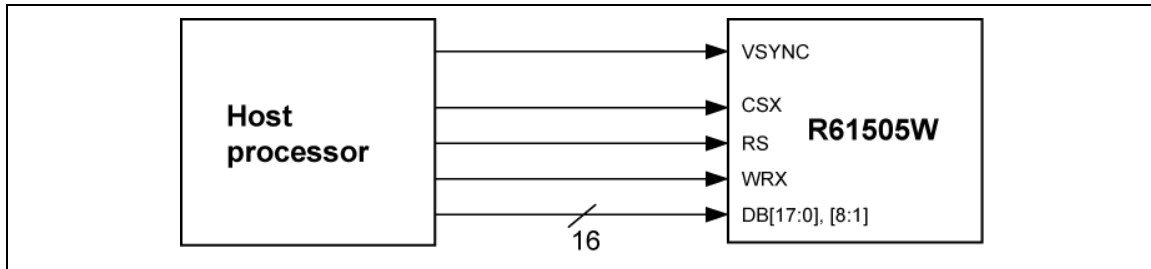


Figure 29 VSYNC Interface

The VSYNC interface is selected by setting $DM[1:0] = 10$ and $RM = 0$. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal frame memory at faster than the calculated minimum speed (internal display operation speed + margin), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal frame memory so that the R61505W rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display.

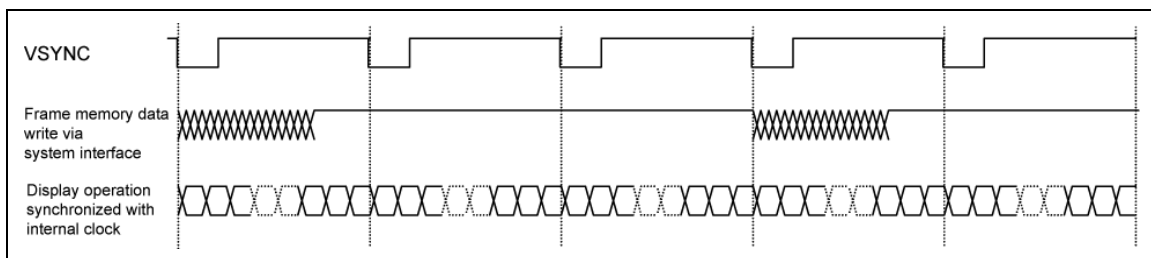


Figure 30 Moving Picture Data Transfers via VSYNC Interface

The VSYNC interface has the minimum for frame memory data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$\begin{aligned} & \text{Internal clock frequency (fosc) [Hz]} \\ & = \text{FrameFrequency} \times (\text{DisplayLines(NL)} + \text{FrontPorch(FP)} + \text{BackPorch(BP)}) \times 16(\text{clocks}) \times \text{variance} \end{aligned}$$

$$\text{FrameMemoryWriteSpeed(min.) [Hz]} > \frac{240 \times \text{DisplayLines(NL)}}{((\text{BackPorch(BP)} + \text{DisplayLines(NL)} - \text{margin}) \times \text{DivisionRatio} \times \text{ClockPer1H}) \times \frac{1}{fosc}}$$

Note: When frame memory write operation does not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of frame memory write operation must also be taken into account.

An example of calculating minimum frame memory writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

| | |
|--|---|
| Panel size | 240 RGB × 320 lines (NL = 6'h27: 320 lines) |
| Total number of lines (NL) | 320 lines |
| Back/front porch | 13/3 lines (BP = 8'h'D, FP = 8'h3) |
| Frame frequency | 60 Hz |
| Maximum internal oscillation frequency | 600 kHz × 1.07 = 642 kHz |
| Clock division ratio (DIVE) | 1 |
| Number of clock per 1H period (RTNE) | 30 |

RTN*: RTNI or RTNE. DIV*: DIVI or DIVE.

- Notes: 1. When the internal clock frequency is set, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±7% for variances and guarantee that display operation is completed within one VSYNC cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for frame memory write [Hz]

$$> 240 \times 320 / \{(13 + 320 - 2) \text{ lines} \times 1 \times 30 \text{ clocks}\} \times 1/642 \text{ kHz} = 4.97 \text{ MHz}$$

- Notes: 1. In this example, it is assumed that the R61505W starts writing data in the internal frame memory on the falling edge of VSYNC.
2. There must be at least a margin of 2 lines between the line to which the R61505W has just written data and the line where display operation on the LCD is performed.

In this example, the frame memory write operation at a speed of 4.97MHz or faster, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before the R61505W starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

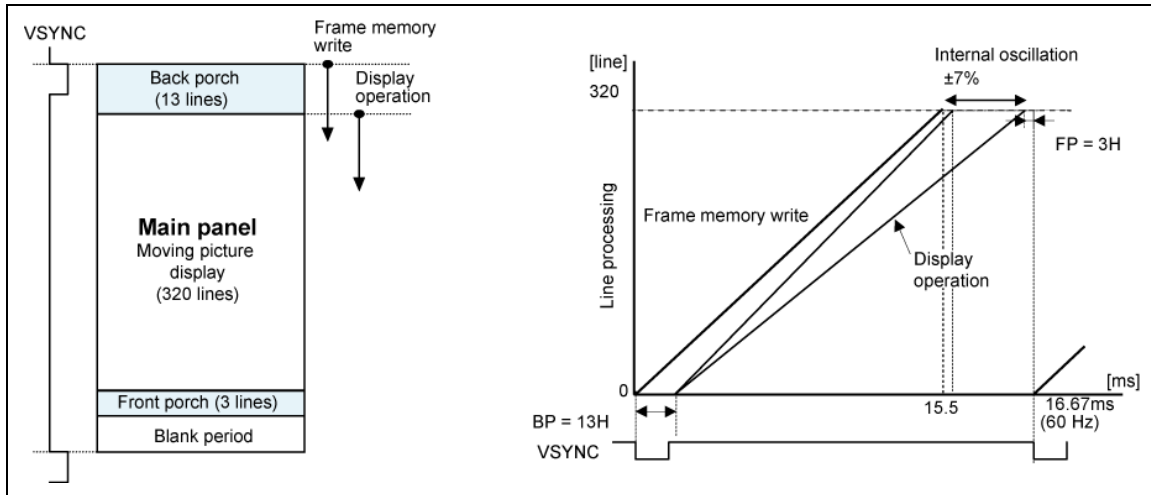


Figure 31 Write/Display Operation Timing via VSYNC Interface

Notes to VSYNC Interface Operation

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margin in setting frame memory write speed for VSYNC interface operation.
2. The above example shows the values when writing over the full screen. Extra margin will be created if the moving picture display area is smaller than that.

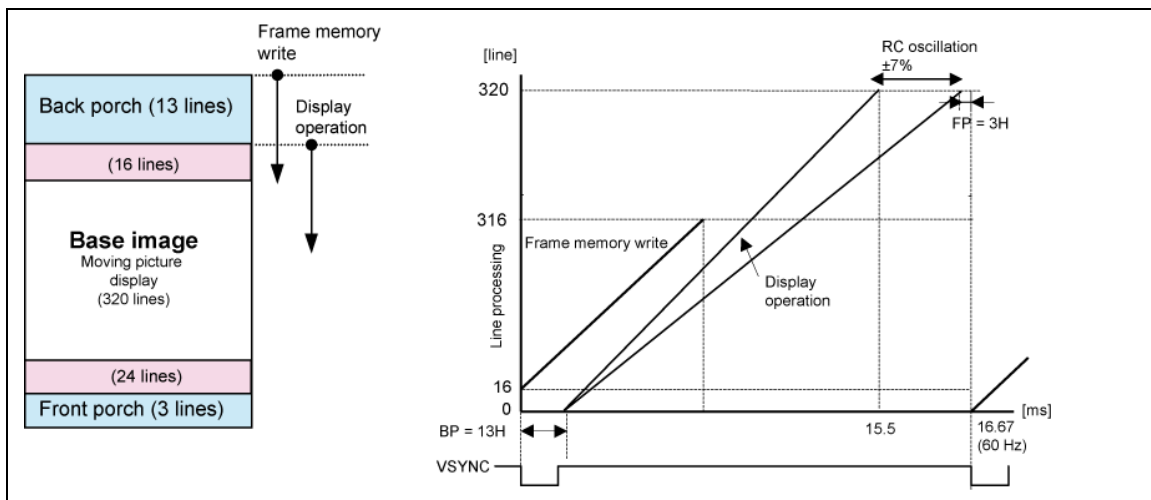


Figure 32 Frame Memory Write Speed Margins

3. The front porch period continues from the end of one frame period to the next VSYNC input.
4. The instructions to switch from internal clock operation ($DM[1:0] = 00$) to VSYNC interface operation modes and vice versa are enabled from the next frame period.
5. The partial display and vertical scroll functions are not available in VSYNC interface operation.
6. In VSYNC interface operation, set $AM = 0$ to transfer display data correctly.

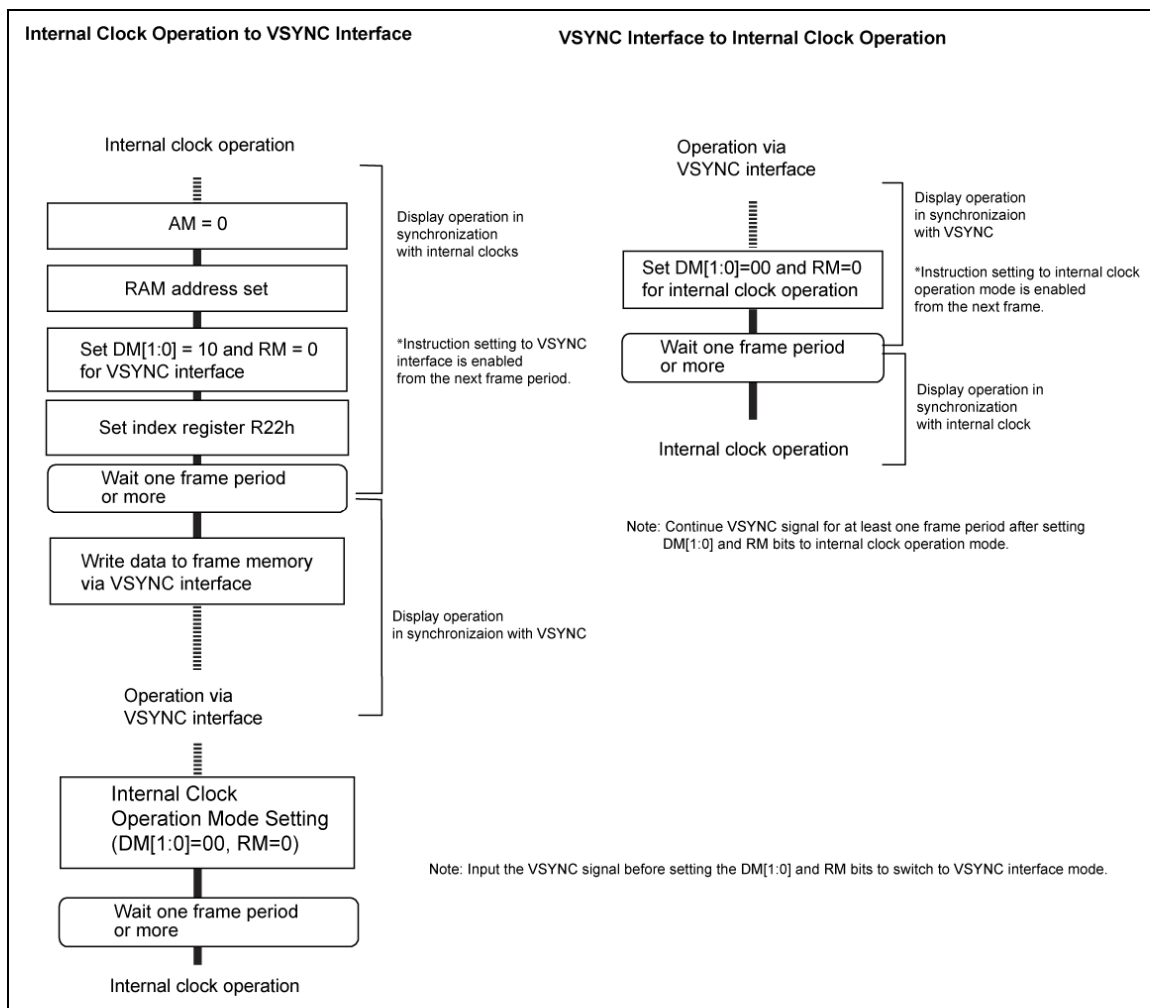


Figure 33 Sequences to Switch between VSYNC and Internal Clock Operation Modes

FMARK Interface

In the FMARK interface operation, data is written to internal frame memory via system interface synchronizing with the frame mark signal (FMARK), realizing tearing less video image while using conventional system interface. FMARK output position is set in units of line using FMP bit. Set the bit considering data transfer speed.

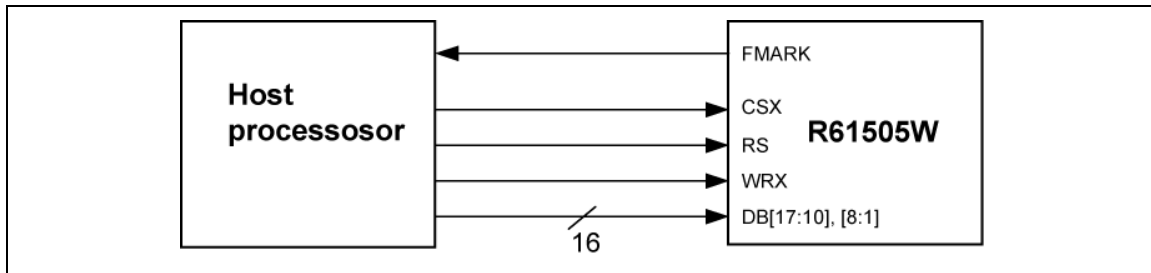


Figure 34 Display Synchronous Data Transfer Interface

In this operation, moving picture display is enabled via system interface by writing data at higher than the internal display operation frequency to a certain degree, which guarantees rewriting the moving picture frame memory area without causing flicker on the display.

The data is written in the internal frame memory. Therefore, when moving picture is displayed, data is written only to the moving picture display area without using RGB or VSYNC interface, minimizing number of data transfer required for moving picture display.

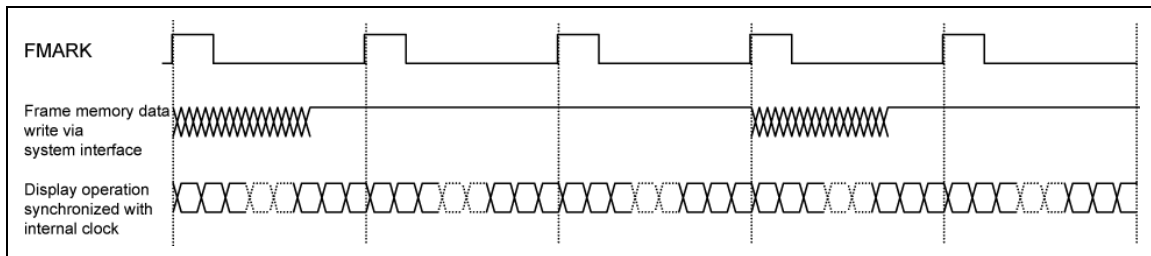


Figure 35 Moving Picture Data Transfers via FMARK Function

When transferring data in synchronization with FMARK signal, minimum frame memory data write speed must be taken into consideration. They must be more than the values calculated from the following equations.

$$FrameMemoryWriteSpeed(\text{min.})[\text{Hz}] > \frac{240 \times DisplayLines(NL)}{(FP + BP) + DisplayLines(NL) - m \text{ args} \times DivisionRatio(DIVE) \times ClockPer1H(RTNE)} \times \frac{1}{fosc}$$

Notes: When frame memory write operation is not started immediately following the rising edge of FMARK, the time from the rising edge of FMARK until the start of frame memory write operation must also be taken into account. RTN*: RTNI or RTNE. DIV*: DIVI or DIVE.

Examples of calculating minimum frame memory data write speed is as follows. The above calculation shows frame memory write speed per 1 pixel and is different from write speed defined by data transfer format of each interface.

[Example]

| | |
|--------------------------------------|---|
| Panel size | 240 RGB × 320 lines |
| Total number of lines (NL) | 320 lines |
| Back/front porch | 13/3 lines (BP = 8h'D, FP = 8'h3) |
| Frame marker position (FMP) | Display end line (320 th line) |
| Frame frequency | 60 Hz |
| Maximum internal operation clock | 600kHz × 1.07 = 642kHz |
| Clock division ratio (DIVE) | 1 |
| Number of clock per 1H period (RTNE) | 30 |

- Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±7% for variances and guarantee that display operation is completed within one FMARK cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for frame memory write [Hz]

$$> 240 \times 320 / \{(13 + 320 - 2) \text{ lines} \times 1 \times 30 \text{ clocks}\} \times 1/642 \text{ kHz} = 4.95 \text{ MHz / pixel}$$

- Notes: 1. In this example, it is assumed that the R61505W starts writing data in the internal frame memory on the rising edge of FMARK.
2. There must be at least a margin of 2 lines between the line to which the R61505W has just written data and the line where display operation on the LCD is performed.
3. The FMARK signal output position is set to the line specified by register.

In this example, frame memory write operation at a speed of 4.95MHz/pixel or faster, when starting on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the R61505W starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

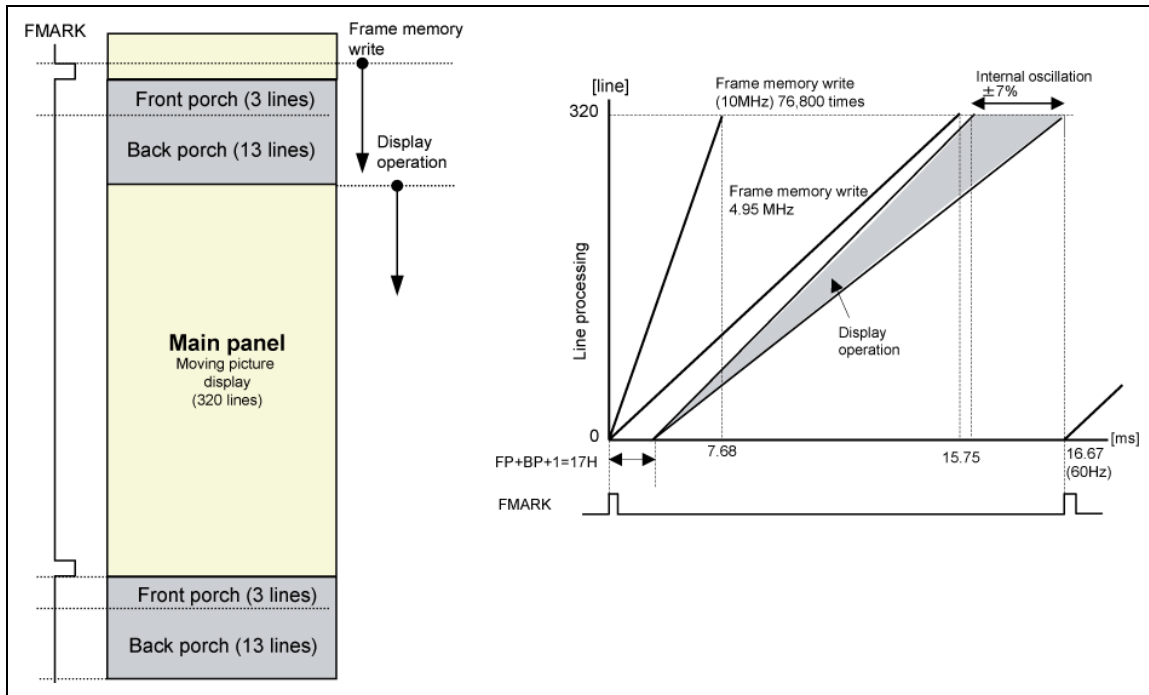


Figure 36

Note to display operation synchronous data transfer using FMARK signal

The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margin in setting frame memory write speed for this operation.

FMP Bit Setting

The host processor detects FMARK signal outputted at the position defined by FMP bit. The R61505W outputs an FMARK pulse when the R61505W is driving the line specified by FMP[8:0] bits. The FMARK signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

The FMARK output interval is set by FMI[2:0] bits. Set FMI[2:0] bits in accordance with display data rewrite cycle and data transfer rate. This setting is enabled when FMARKOE = 1.

Table 67

| FMP[8:0] | FMARK output position |
|--------------|------------------------|
| 9'h000 | 0 |
| 9'h001 | 1 st line |
| 9'h002 | 2 nd line |
| : | : |
| 9'h14D | 333 rd line |
| 9'h14E | 334 th line |
| 9'h14F | 335 th line |
| 9'h150 ~ 1FF | Setting disabled |

Table 68

| FMI[2] | FMI[1] | FMI[0] | FMARK output interval |
|---------------|--------|--------|-----------------------|
| 0 | 0 | 0 | 1 frame period |
| 0 | 0 | 1 | 2 frame periods |
| 0 | 1 | 1 | 4 frame periods |
| 1 | 0 | 1 | 6 frame periods |
| Other setting | | | Setting disabled |

FMP Setting Example

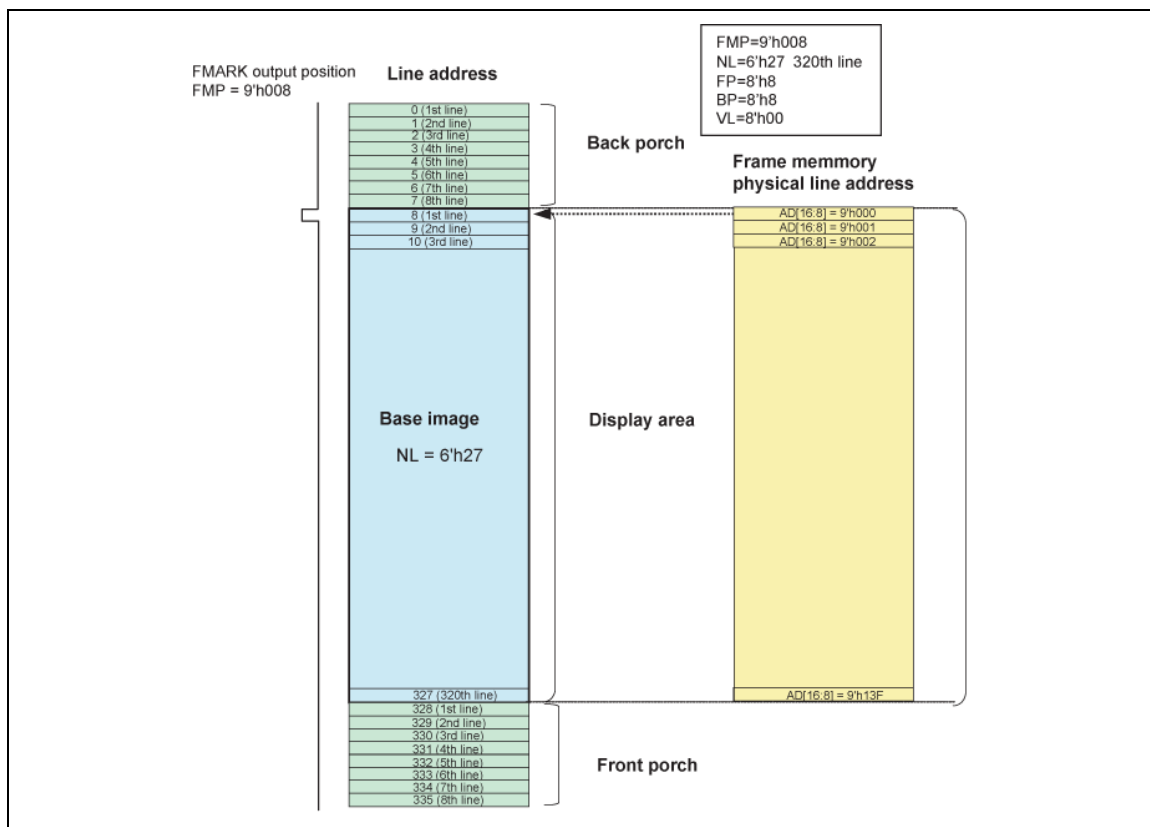


Figure 37

External Display Interface

The R61505W supports the RGB interface. The interface format is set by RM[1:0] bits. The internal frame memory is accessible via RGB interface.

Table 69 RGB Interface

| RIM1 | RIM0 | RGB interface | DB pin |
|------|------|----------------------|---------------------|
| 0 | 0 | 18-bit RGB interface | DB[17:0] |
| 0 | 1 | 16-bit RGB interface | DB[17:13], DB[11:1] |
| 1 | 0 | Setting inhibited | - |
| 1 | 1 | Setting inhibited | - |

Note: Using more than two interfaces at a time is prohibited.

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The data can be written only within the specified area with low power consumption by using window address function. In RGB interface operation, front and back porch periods must be made before and after the display period.

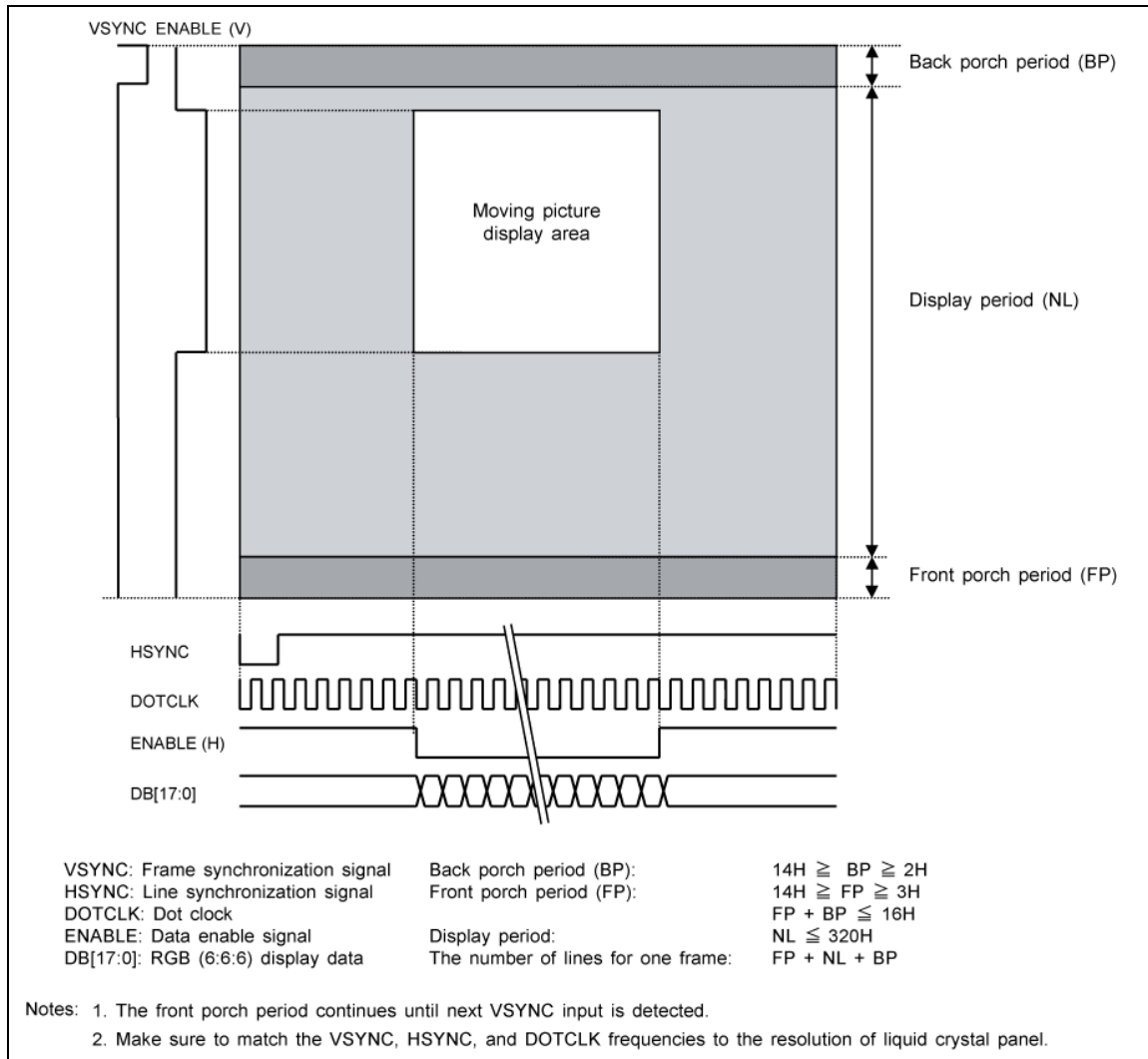


Figure 38 Display Operation via RGB Interface

Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals

The polarities of VSYNC, HSYNC, ENABLE, and DOTCLK signals can be changed by setting the DPL, EPL, HSPL, and VSPL bits respectively for convenience of system configuration.

RGB Interface Timing

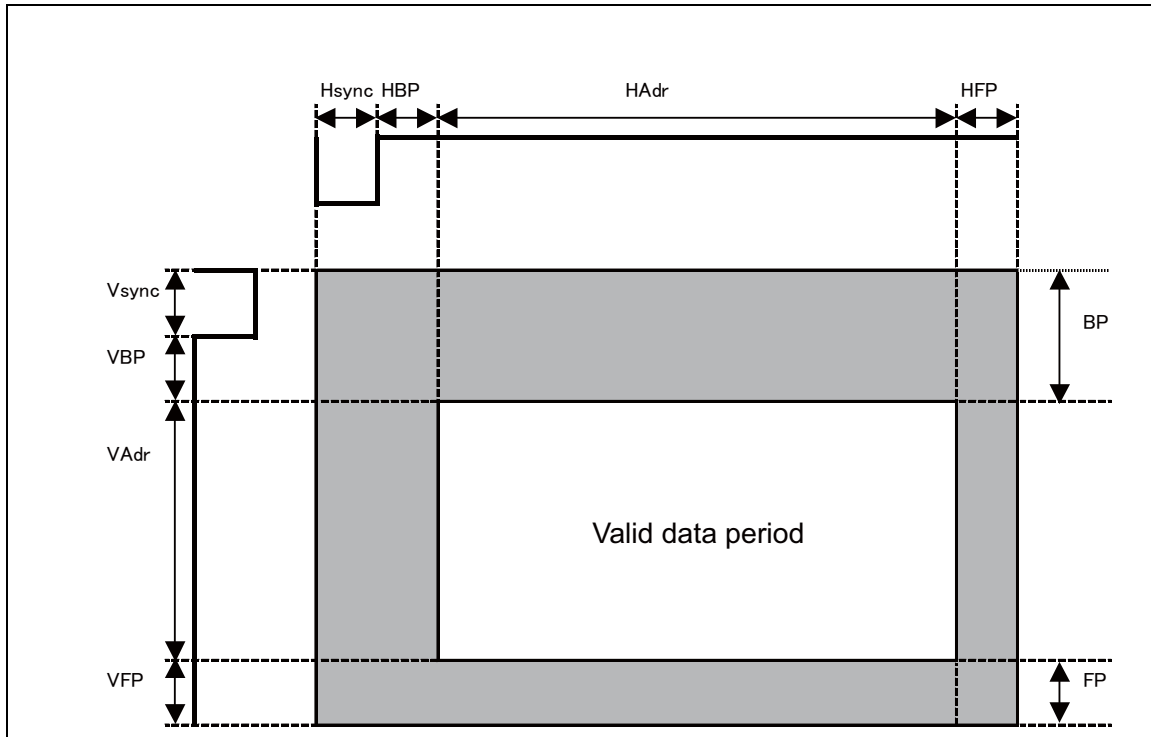


Figure 39

Table 70

| Parameters | Symbols | Min. | Typ. | Max. | Step | Unit |
|----------------------------|---------|------|------|------|------|-----------|
| Horizontal Synchronization | Hsync | 2 | 10 | 16 | 1 | DOTCLKCYC |
| Horizontal Back Porch | HBP | 2 | 20 | 24 | 1 | DOTCLKCYC |
| Horizontal Address | HAdr | — | 240 | — | 1 | DOTCLKCYC |
| Horizontal Front Porch | HFP | 2 | 10 | 16 | 1 | DOTCLKCYC |
| Vertical Synchronization | Vsync | 1 | 2 | 4 | 1 | Line |
| Vertical Back Porch | VBP | 1 | 2 | — | 1 | Line |
| Vertical Address | VAdr | — | 320 | — | 1 | Line |
| Vertical Front Porch | VFP | 3 | 4 | — | 1 | Line |

Notes: 1. Typ. is the setting example under the following usage conditions (resolution of the panel = QVGA 240 x 320, clock frequency = 5.64 MHz, frame frequency = about 60 Hz).

2. In case of setting, make sure (Number of DOTCLK in 1H period) \geq RTNE[5:0] (number of clocks) \times DIVE[1:0] (Division ratio) \times (PCDIVL + PCDIVH). The setting example is shown in next page.

Setting Example of Display Control Clock in RGB Interface Operation

Register

The display operation is performed by the internal clock (DOTCLKD) generated by dividing the frequency of DOTCLK.

PCDIVH[2:0] defines number of DOTCLK during DOTCLKD is high in the units of 1clock.

PCDIVL[2:0] defines number of DOTCLK during DOTCLKD is low in the units of 1clock.

Also, write PCDIVH and PCDIVL values so that DOTCLKD frequency is the closest to internal oscillation clock frequency (600 KHz). Make sure that $PCDIVL = PCDIVH$ or $PCDIVH - 1$. Make sure that (number of DOTCLKs in 1H) \geq RTNE (number of clocks) * DIVE (division ratio) * (PCDIVL + PCDIVH).

Setting example: in case of setting the frame frequency to 60Hz

Internal clock: Internal oscillation clock = 600 kHz
 DIVE = 2'b0 (1/1)
 RTNE = 30 clocks
 FP = 8'h8, BP = 8'h8, NL = 6'h27 (320 lines)
 \rightarrow 59.52Hz

DOTCLK: Hsync = 10 clocks
 HBP = 20 clocks
 HFP = 10 clocks
 $60\text{Hz} \times (8+320+8) \text{ lines} \times (10+20+240+10) \text{ clocks} = 5.64\text{MHz}$
 DOTCLK frequency = 5.64MHz
 $5.64\text{MHz} / 600\text{kHz} = 9.4 \rightarrow$ Write PCDIVH and PCDIVL values so that DOTCLK frequency is divided into 9.
 $5.64 / 9 = 6.27 \text{ kHz}$
 $(627 \text{ kHz} / 1) / 30 \text{ clocks} / 336 \text{ lines} = 62.2\text{Hz}$

PCDIVH: 3'h4

PCDIVL: 3'h4

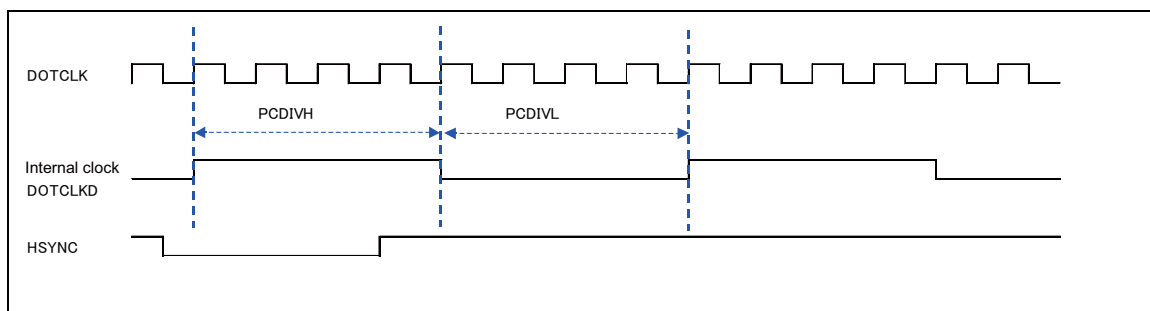


Figure 40

RGB Interface Timing

The timing relationship of signals in RGB interface operation is as follows.

16-/18-Bit RGB Interface Timing

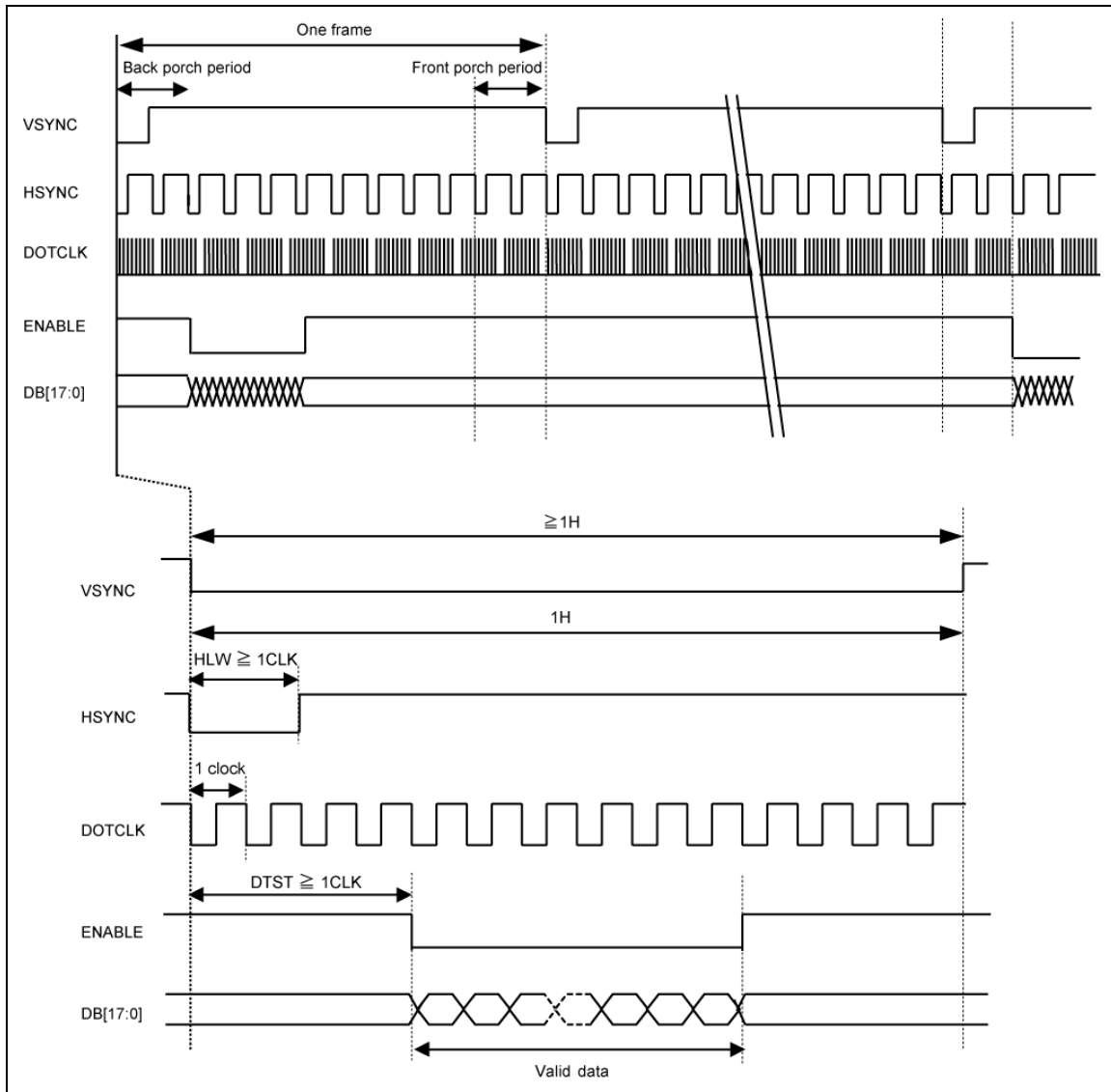


Figure 41

Note: VLW: VSYNC Low period
 HLW: HSYNC Low period
 DTST: Data transfer setup time

Moving Picture Display via RGB Interface

The R61505W supports RGB interface for moving picture display and incorporates frame memory for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function enables transferring data only within the moving picture area
2. It becomes possible to transfer only the data written over the moving picture area
3. By reducing data transfer, it can contribute to lowering the power consumption of the whole system
4. The data in still picture area (icons etc.) can be written over via system interface while displaying a moving picture via RGB interface

Frame Memory Access via System Interface in RGB Interface Operation

The R61505W allows frame memory access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal frame memory in synchronization with DOTCLK while ENABLE is “Low”. When writing data to the frame memory via system interface, set ENABLE “High” to stop writing data via RGB interface. Then set RM = “0” to enable frame memory access via system interface. When reverting to the RGB interface operation, wait for the read/write bus cycle time. Then, set RM = “1” and the index register to R22h to start accessing frame memory via RGB interface. If there is a conflict between frame memory accesses via two interfaces, there is no guarantee that the data is written in the frame memory.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

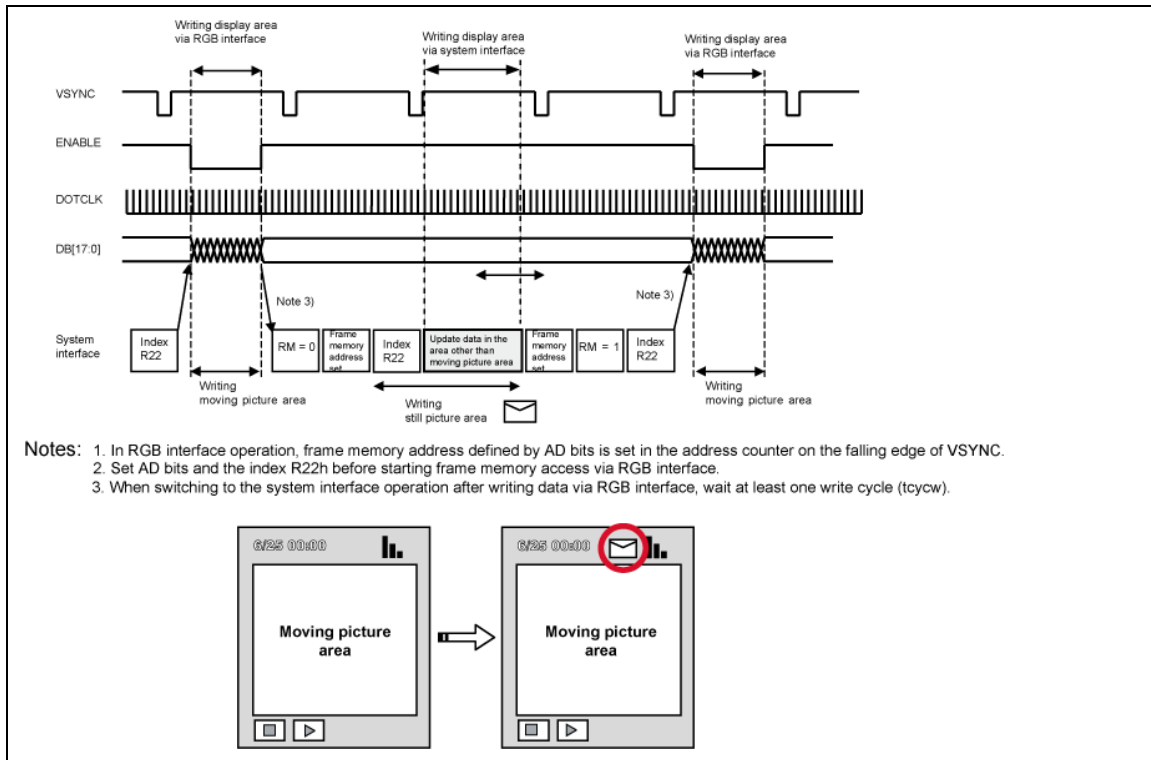


Figure 42 Updating the Still Picture Area while Displaying Moving Picture

16-Bit RGB Interface

The 16-bit RGB interface is selected by setting RIM[1:0] = 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal frame memory in synchronization with the display operation via 16-bit ports while data enable signal (ENABLE) allows frame memory access via RGB interface.

Instruction bits can be transferred only via system interface.

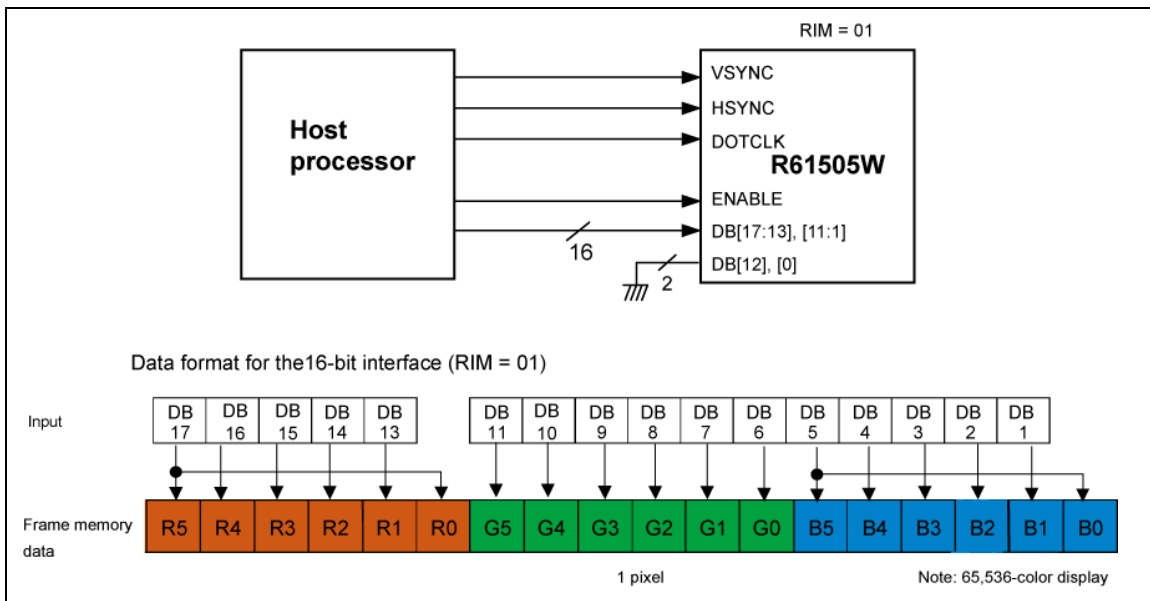


Figure 43 Example of 16-Bit RGB Interface and Data Format

18-Bit RGB Interface

The 18-bit RGB interface is selected by setting RIM[1:0] = 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal frame memory in synchronization with the display operation via 18-bit ports (DB[17:0]) while data enable signal (ENABLE) allows frame memory access via RGB interface.

Instruction bits can be transferred only via system interface.

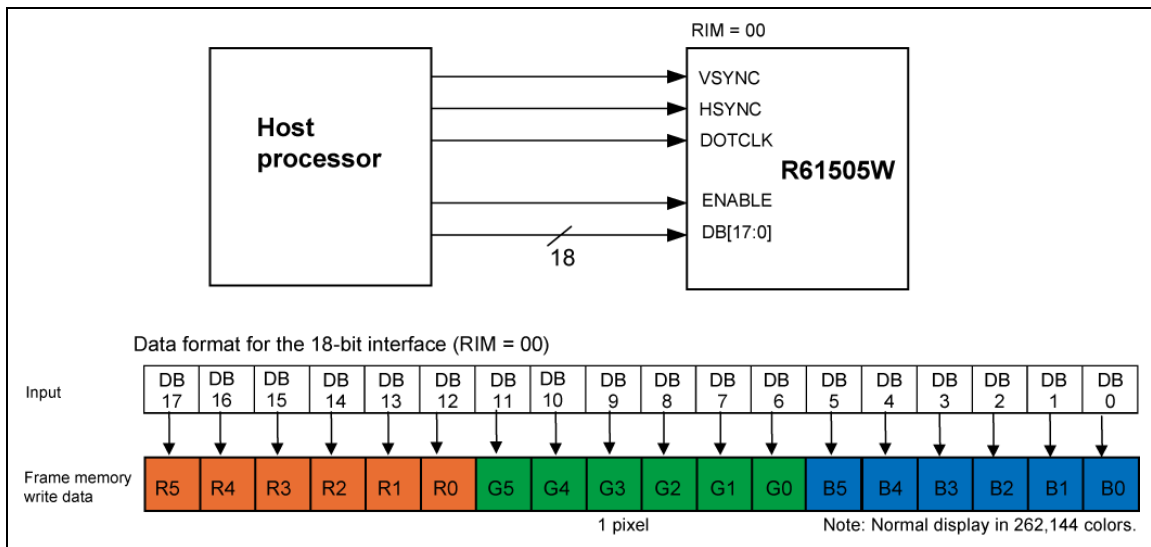


Figure 44 Example of 18-Bit RGB Interface and Data Format

Notes on RGB Interface Operation

a. The following functions are not available in external display interface operation.

Table 71 Functions Not Available in External Display Interface Operation

| Function | External display interface | Internal display operation |
|-----------------|----------------------------|----------------------------|
| Partial display | Not available | Available |
| Scroll function | Not available | Available |

b. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.

c. The reference clock to generate liquid crystal panel controlling signals in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.

d. When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

e. In RGB interface operation, front porch period continues after the end of frame period until next VSYNC input is detected.

f. In RGB interface operation, frame memory address AD[16:0] is set in the address counter every frame on the falling edge of VSYNC.

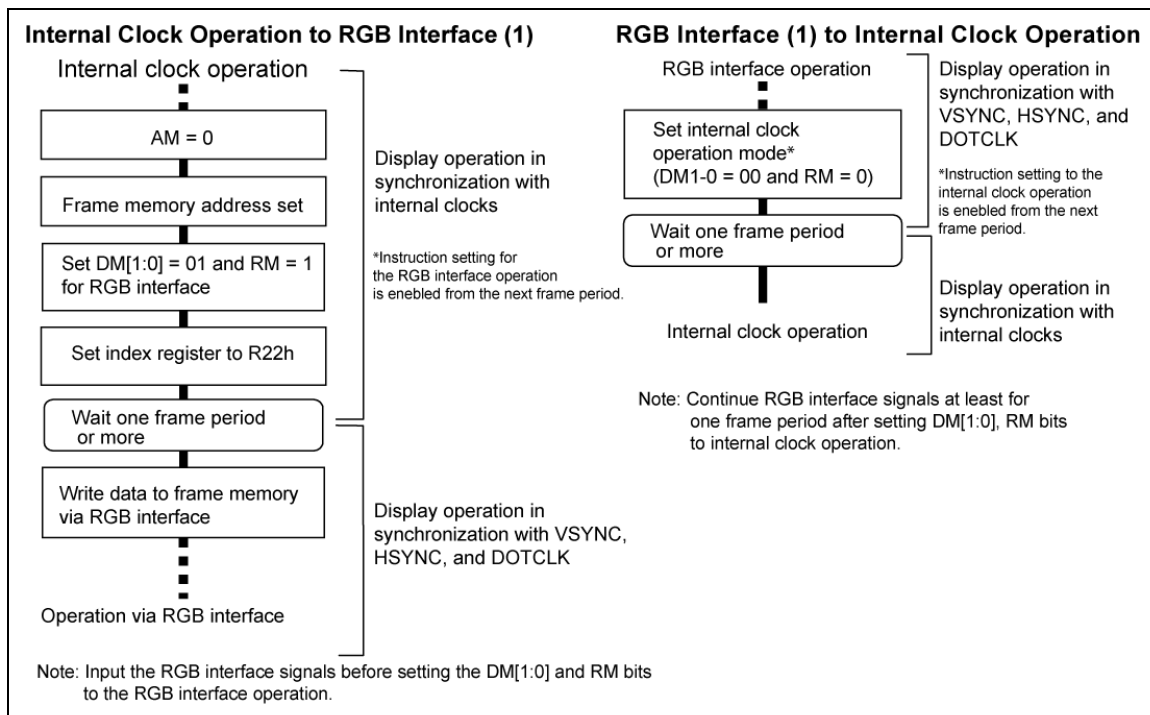


Figure 45 RGB and Internal Clock Operation Mode Switching Sequences

Frame Memory Address and Display Position on the Panel

The R61505W has memory to store display data of 240RGB x 320 lines. The R61505W incorporates a circuit to control partial display, which allows switching driving method between full-screen display mode and partial display mode.

The R61505W makes display arrangement setting and panel driving position control setting separately and specifies frame memory area for each image displayed on the panel. For this reason, there is no need to take the mounting position of the panel into consideration when designing a display on the panel.

The following is the sequence of setting full-screen and partial display.

1. Set PTSA and PTEA bits to specify the frame memory area for a partial image
2. Set the display position of the partial image on the base image by setting PTDP.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE and PTDE) to display images

| | |
|-----------------|---------------------|
| Normal display | BASEE = 1, PTDE=0 |
| Partial display | BASEE = 0, PTDE = 1 |

5. Rewrite BASEE and PTDE bits when switching full display and partial display of the base image.

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, set SS bit when writing frame memory data.

Table 72

| | Display ENABLE | Numbers of lines | Frame memory area |
|------------|----------------|------------------|-------------------------------|
| Base image | BASEE | NL | (BSA, BEA) = (9'h000, 9'h13F) |

Notes 1: The base image is displayed from the first line of the screen.

- 2: Make sure $NL \leq 320 \text{ (lines)} = BEA - BSA$ when setting a base image frame memory area. BSA and BEA are fixed to 9'h000, 9'h13F, respectively.

Table 73

| | Display ENABLE | Display position | Frame memory area |
|---------------|----------------|------------------|-------------------|
| Partial image | PTDE | PTDP | (PTSA, PTEA) |

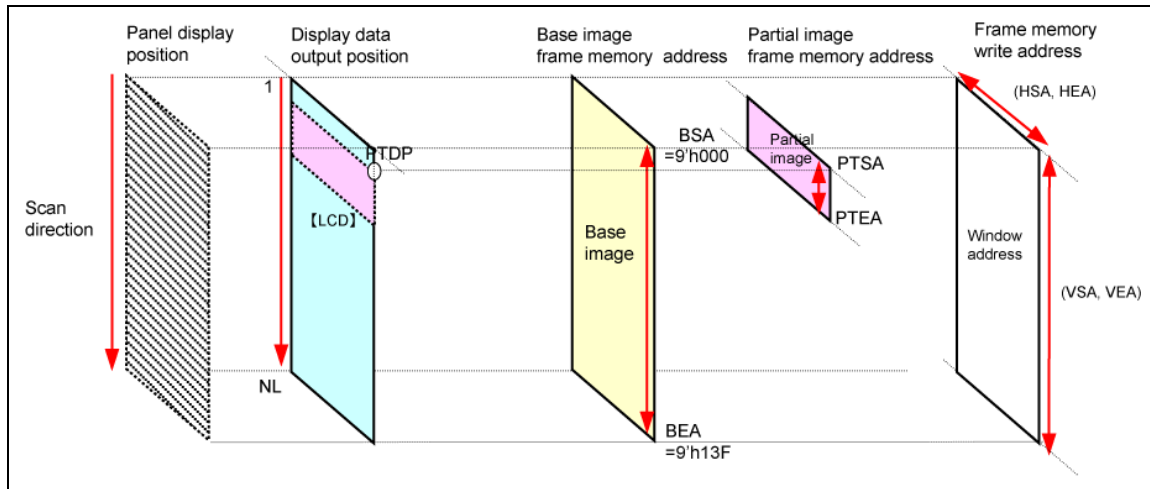


Figure 46 Frame Memory Address, Display Position and Drive Position

Restrictions in Setting Display Control Instruction

There are restrictions in coordinates setting for display data, display position and partial display.

(1) Screen Setting

In setting the number of lines to drive the liquid crystal panel, make sure that the total number of lines is 320 lines or less ($NL \leq 320$ lines).

(2) Base Image Display

1. The base image is displayed from the first line of the screen: $BSA = 1^{\text{st}}$ line (of the display panel)
2. The base image frame memory area (specified by $BSA = 000$, $BEA = 13F$) must include the same or more number of lines set by NL bits (liquid crystal panel drive lines): $BEA - BSA = 320 \text{ lines} \geq NL$

The following figure shows the relationship among the frame memory address, display position, and the lines driven for the display.

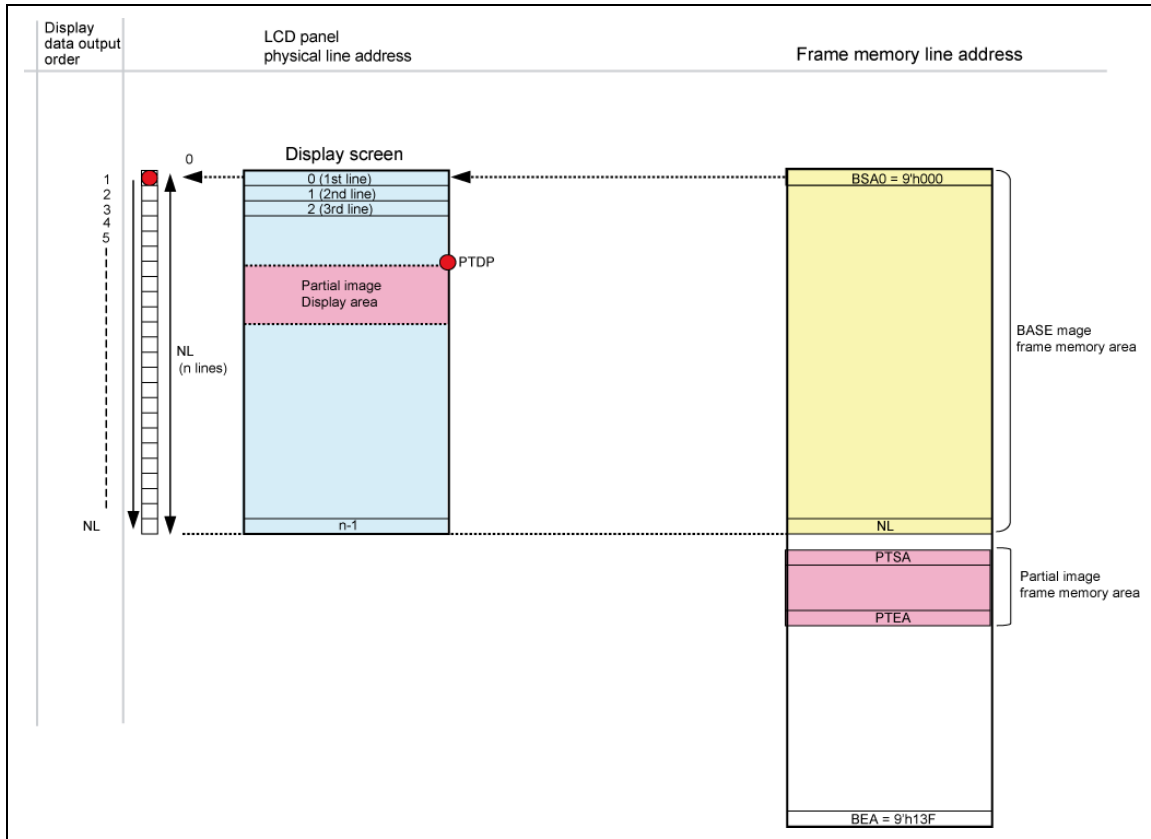


Figure 47 Display Frame Memory Address and Panel Display Position

Note: This figure shows the relationship between frame memory line address and the display position on the panel. In the R61505W's internal operation, the data is written in the frame memory area specified by the window address setting registers.

Instruction Setting Example

The followings are examples of settings for 240 (RGB) x 320 (lines) panel.

1. Full Screen Display with no Partial Image

The following is an example of settings for full screen display.

Table 74

| Base image display instruction | |
|--------------------------------|-------|
| BASEE | 1 |
| NL[5:0] | 6'h27 |
| | |
| PTDE | 0 |

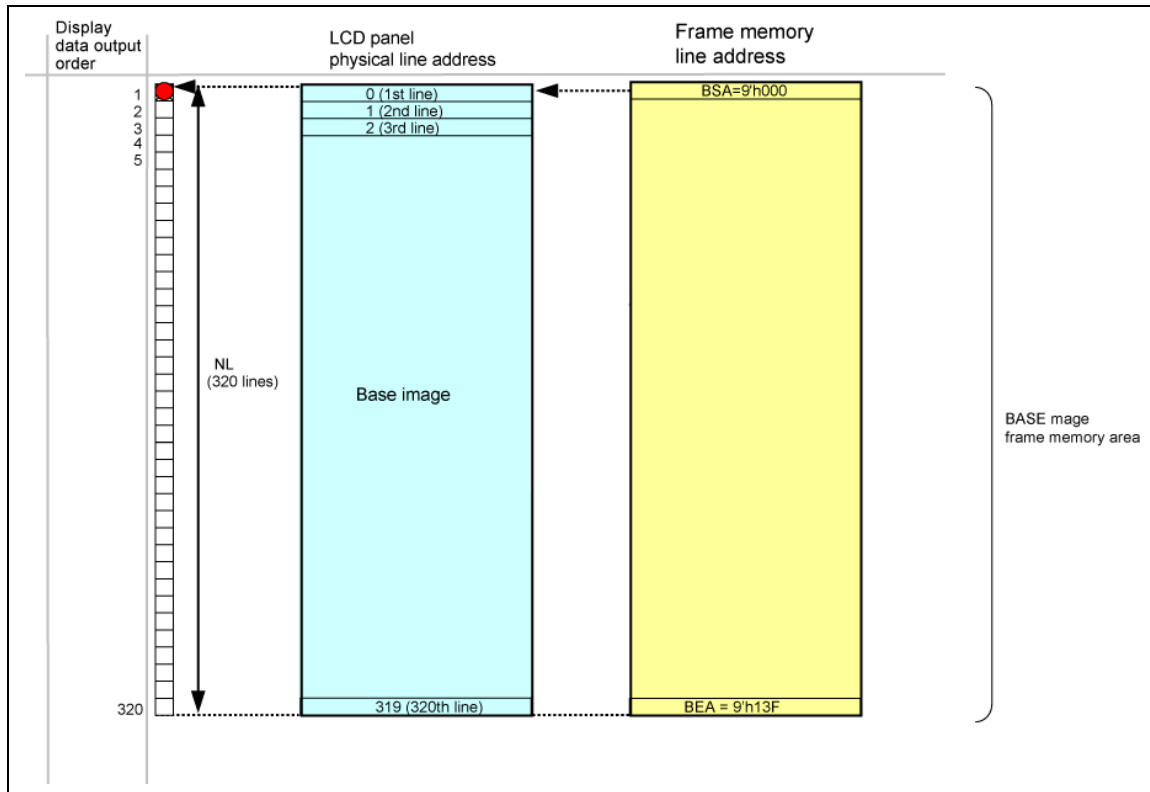


Figure 48 Full Screen Display with no Partial Image

2. Partial Display

The following is an example of settings for displaying only partial image and turning off the base image. The partial image is displayed at the designated position.

Table 75

| Base image display instruction | |
|--------------------------------|-------|
| BASEE | 0 |
| NL[5:0] | 6'h27 |

| Partial image display instruction | |
|-----------------------------------|--------|
| PTDE | 1 |
| PTSA [8:0] | 9'h000 |
| PTEA [8:0] | 9'h00F |
| PTDP [8:0] | 9'h080 |

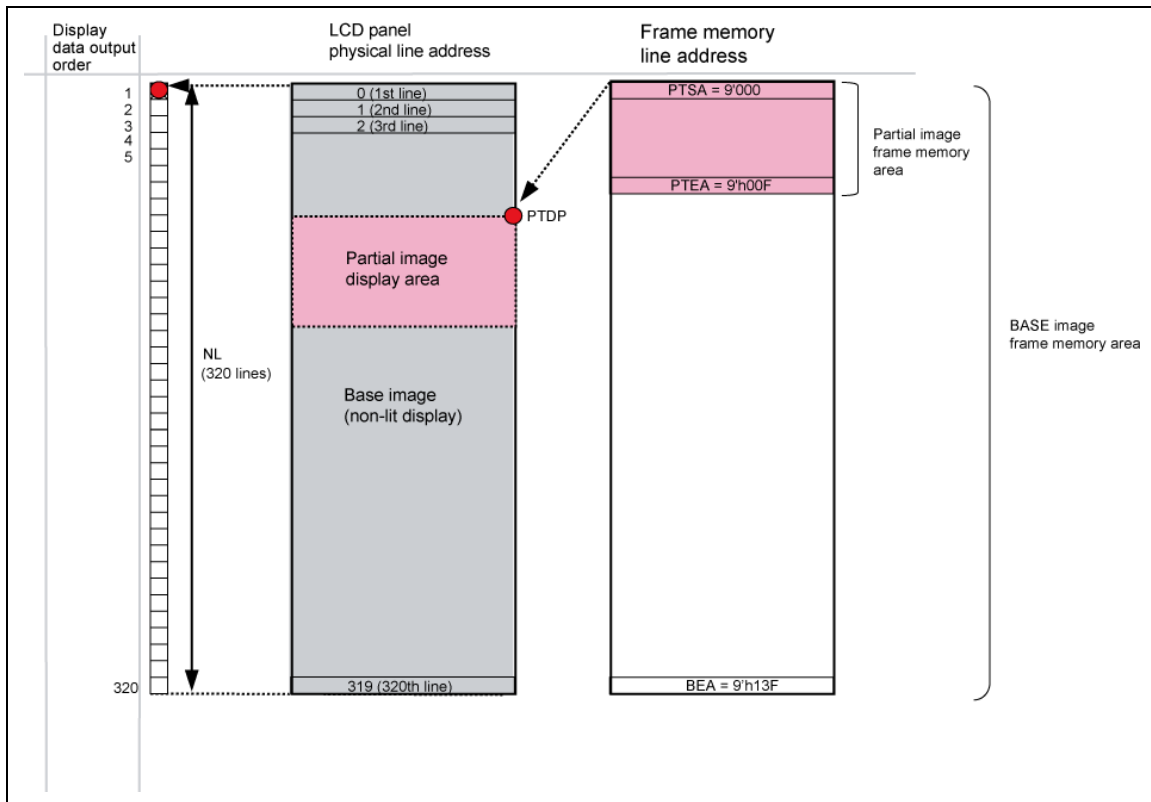


Figure 49 Partial Display

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal frame memory. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[8:0], end: VEA[8:0] bits). The AM and I/D bits set the transition direction of frame memory address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the R61505W to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the frame memory address map area. Also, the AD[16:0] bits (frame memory address set register) must be set to an address within the window address area.

| | |
|--------------------------------------|---|
| [Window address area setting range] | |
| (Horizontal direction) | $8'h00 \leq HSA < HEA \leq 8'hEF$ |
| (Vertical direction) | $9'h000 \leq VSA < VEA \leq 9'h13F$ |
| [Frame memory Address setting range] | |
| (Frame memory address) | $HSA \leq AD [7:0] \leq HEA$ $VSA \leq AD [16:8] \leq VEA$ |

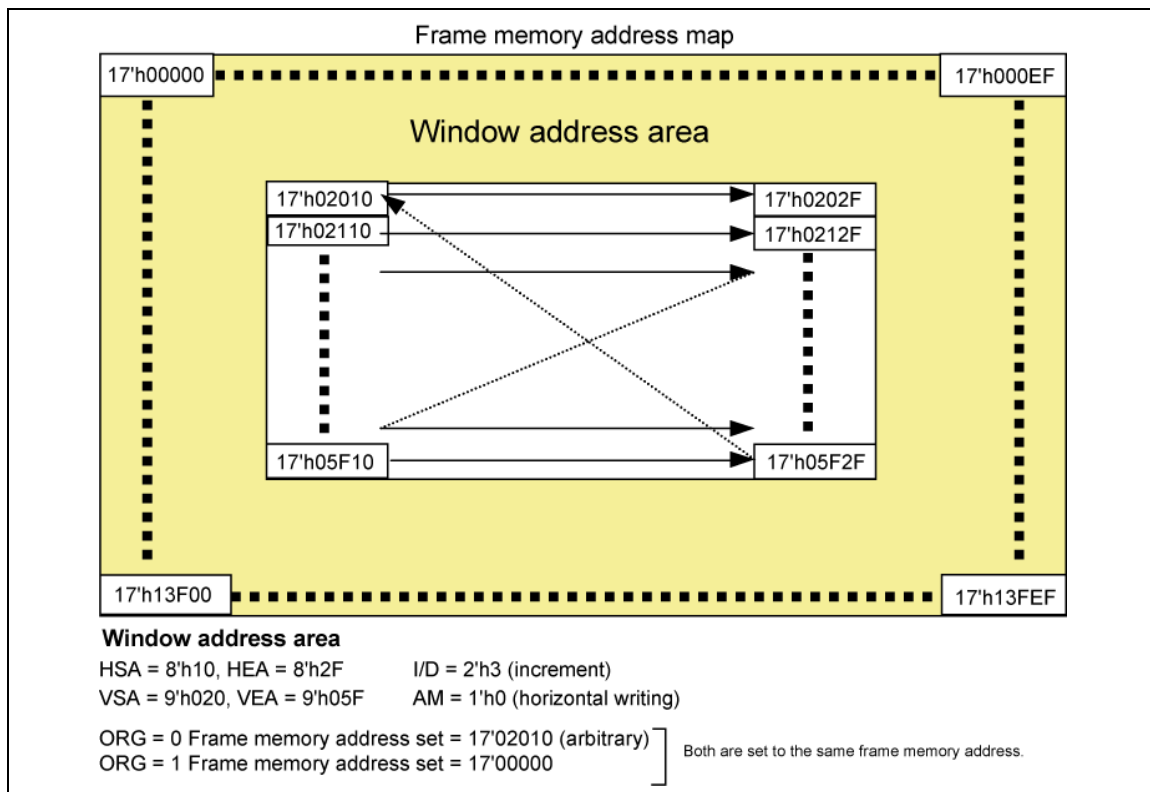


Figure 50 Automatic Address Update within a Window Address Area

Scan Mode Setting

The R61505W can set the gate pin assignment and the scan direction in the following 4 different ways by setting SM and GS bits to realize various connections between the R61505W and the LCD panel.

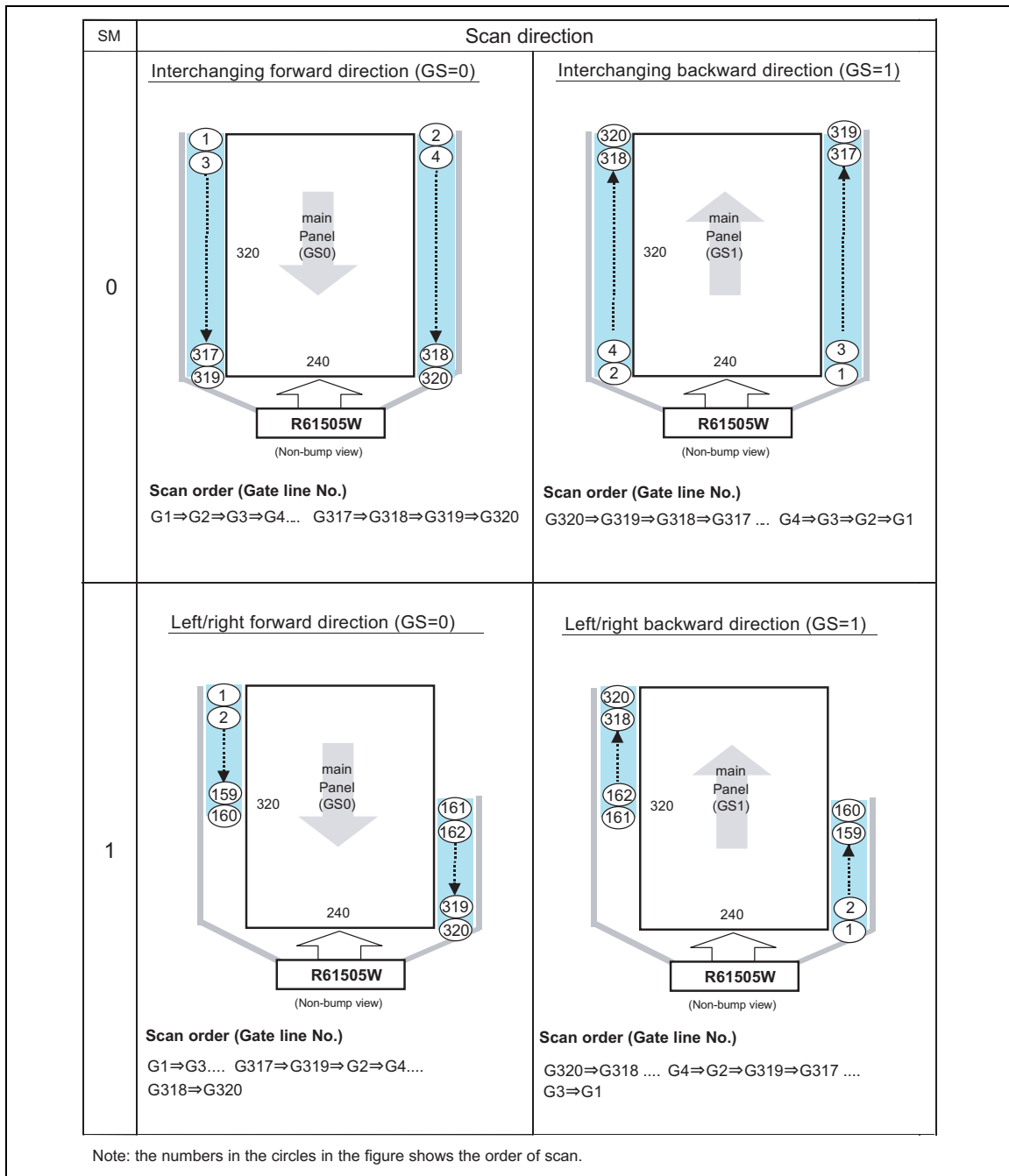


Figure 51

8-Color Display Mode

The R61505W has a function to display in eight colors. In this display mode, only V0 and V63 are used and power supplies to other grayscales (V1 to V62) are turned off to reduce power consumption.

In 8-color display mode, the γ -adjustment registers R30h-R39h are disabled and the power supplies to V1 to V62 halt. The R61505W does not require rewriting frame memory data for 8-color display. Only MSBs of red, green and blue data is used to display image on the panel.

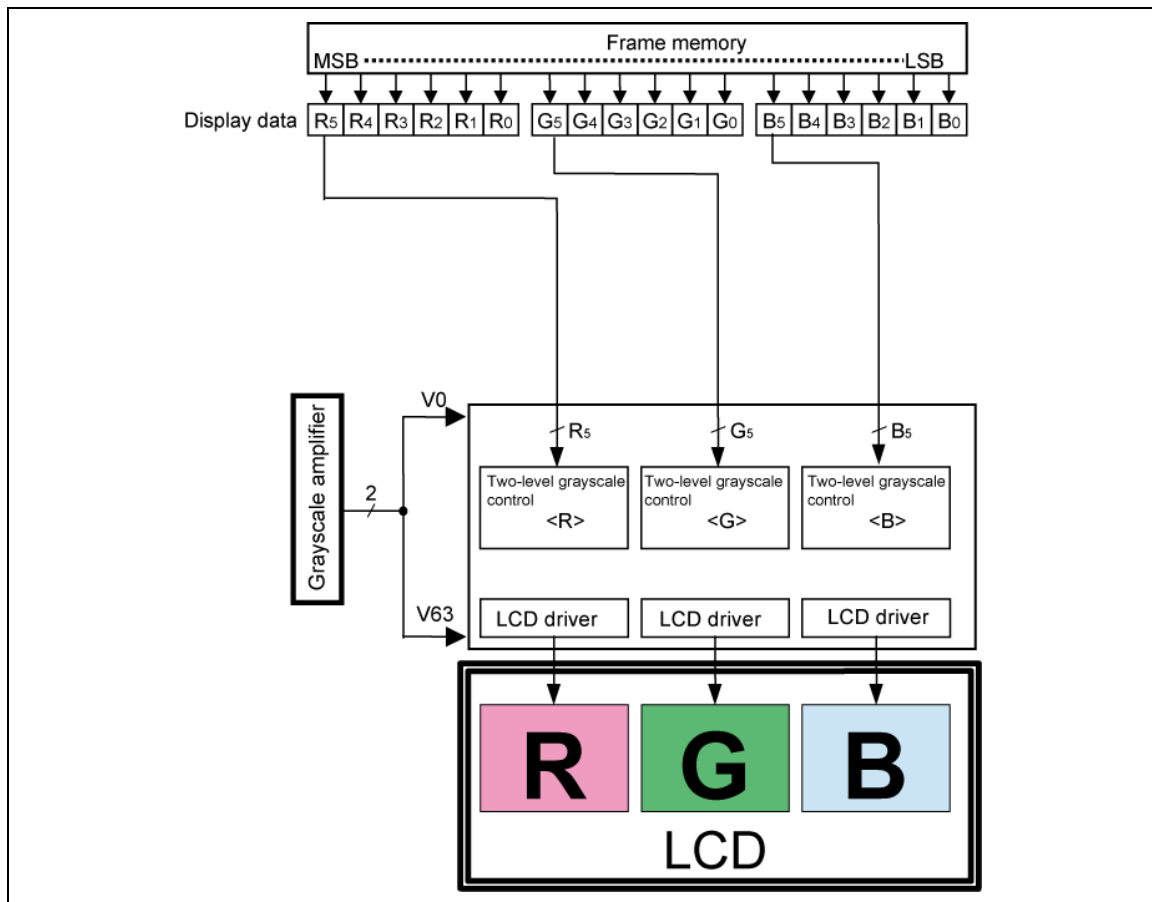


Figure 52 8-Color Display Mode

Line Inversion AC Drive

The R61505W supports n-line inversion alternating current drive in addition to frame-inversion liquid crystal alternating current drive. The timing to invert the electric current can be set to either every line or every two lines. Set line number of inversion timing checking display quality on liquid crystal display. Note that less number of line leads to higher inversion frequency of liquid crystal and more charge/discharge battery in liquid crystal display.

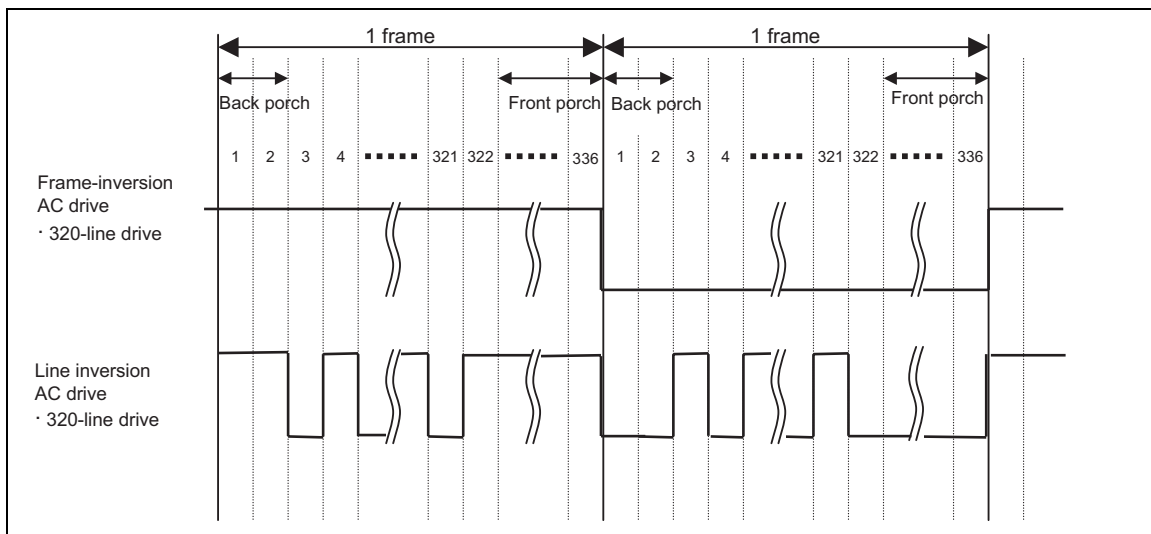


Figure 53 Example of Alternating Signals for N-Line Inversion

Note: Polarity of signals does not invert during blank periods, namely back and front porch periods. N-line inversion operation starts from the first line of a display area.

Alternating Timing

The following figure illustrates the liquid crystal polarity inversion timing in different LCD driving methods. In case of frame-inversion AC drive, the polarity is inverted as the R61505W draws one frame, which is followed by a blank period lasting for (BP+FP) periods. In case of line inversion AC drive, selected by setting BC0=1 (R02h), polarity is inverted as the R61505W draws one line, and a blank period lasting for (BP+FP) periods is inserted when the R61505W draws one frame.

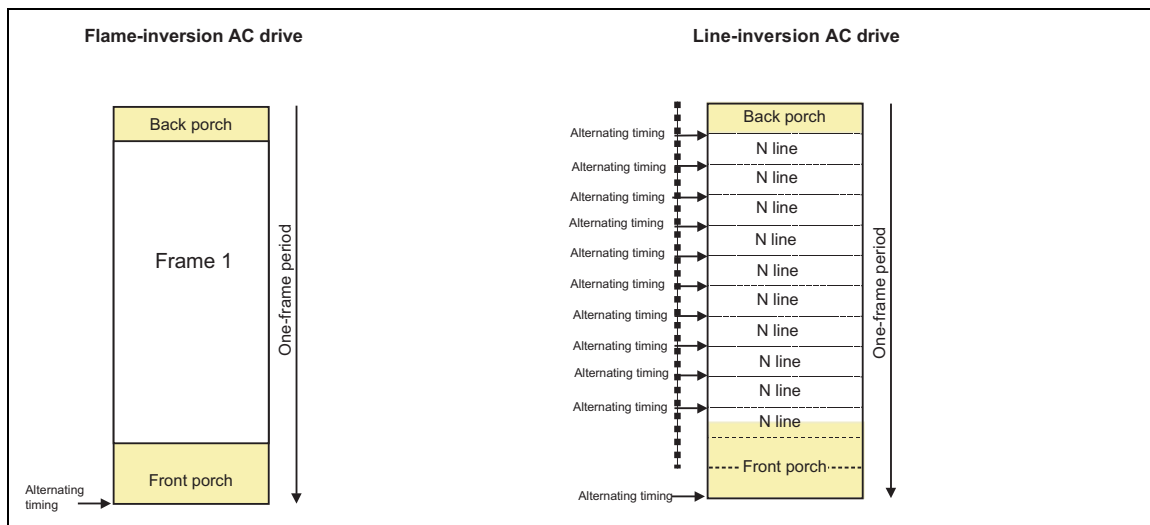


Figure 54 Alternating Timing

Note: Frame inversion AC drive is available only in 8-color display mode. Check the quality of display on the panel.

Frame Frequency Adjustment Function

The R61505W supports a function to adjust frame frequency. The frame frequency for driving liquid crystal can be adjusted by setting the DIV, RTN bits without changing the oscillation frequency.

The R61505W allows changing the frame frequency depending on whether moving picture or still picture is displayed on the screen. In this case, set a high oscillation frequency. By changing the DIVI and RTNI settings, the R61505W can operate at high frame frequency when displaying a moving picture, which requires the R61505W to rewrite data in high speed, and it can operate at low frame frequency when displaying a still picture.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The following equation represents the relationship between liquid crystal drive duty and frame frequency. The frame frequency can be changed by setting the 1H period adjustment bit (RTNI) and the operation clock frequency division ratio setting bit (DIVI).

Equation for calculating frame frequency

$$FrameFrequency(f_{FLM}) = \frac{f_{osc}}{NumberofClocks / line \times DivisionRatio \times (Line + FP + BP)} [Hz]$$

f_{osc} : clock frequency for internal operation (600kHz)

Number of clocks per line: RTNI bit

Division ratio: DIVI bit

Line: number of lines to drive the LCD panel (NL bit)

Number of lines for front porch: FP

Number of lines for back porch: BP

Example of Calculation: when maximum frame frequency = 60 Hz

f_{osc} : 600kHz

Number of lines: 320 lines

1H period: 30 clock cycles (RTNI[4:0] = "1E")

Division ratio of operating clock: 1

Front porch: 8 lines

Back porch: 8 lines

$$f_{FLM} = 600kHz / (30 \text{ clocks} \times 1/1 \times (320 + 8 + 8) \text{ (lines)}) \approx 60Hz$$

Partial Display Function

The partial display function allows the R61505W to drive lines selectively to display partial image by setting partial display control registers. The lines not used for displaying partial images are driven at non-lit display level to reduce power consumption.

The power efficiency can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

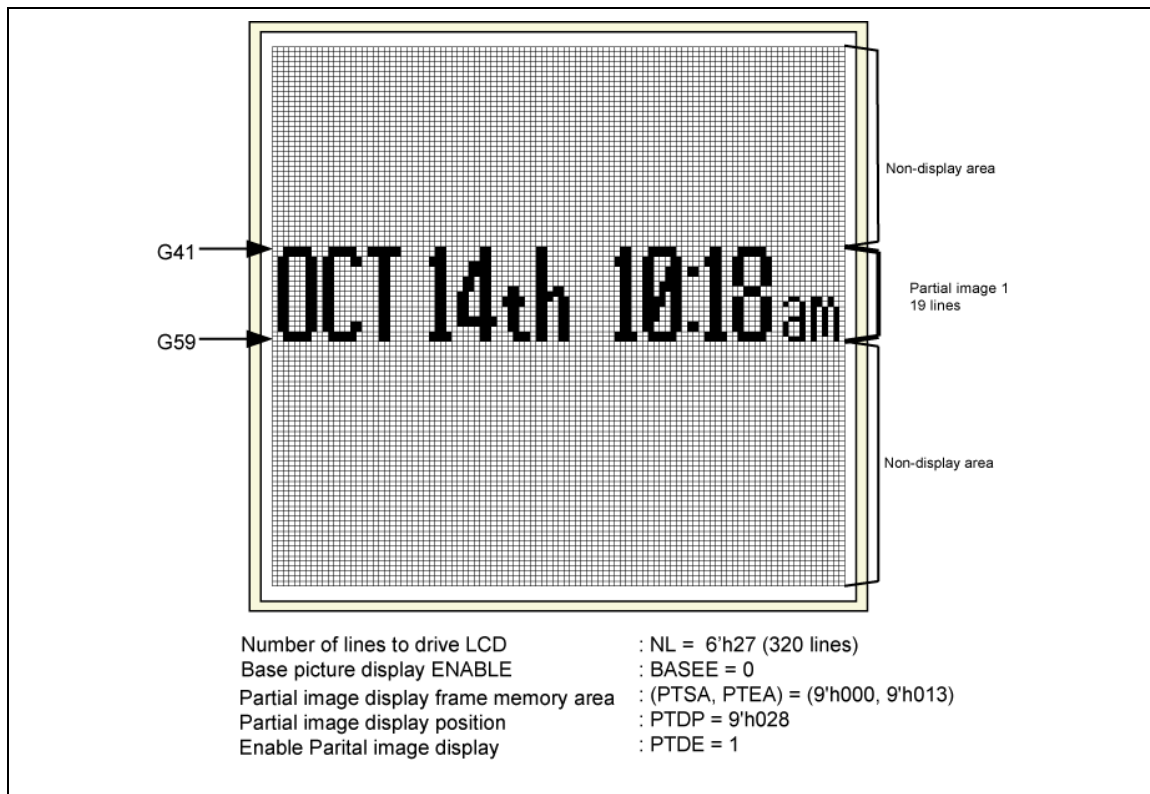


Figure 55 Partial Display Example

Note: See the “Frame Memory Address and Display Position on the Panel” for details on the relationship between the display positions of partial images and respective frame memory area setting.

Liquid Crystal Panel Interface Timing

The relationships between RGB interface signals and liquid crystal panel control signals in internal operation and RGB interface operations are as follows

Internal Clock Operation

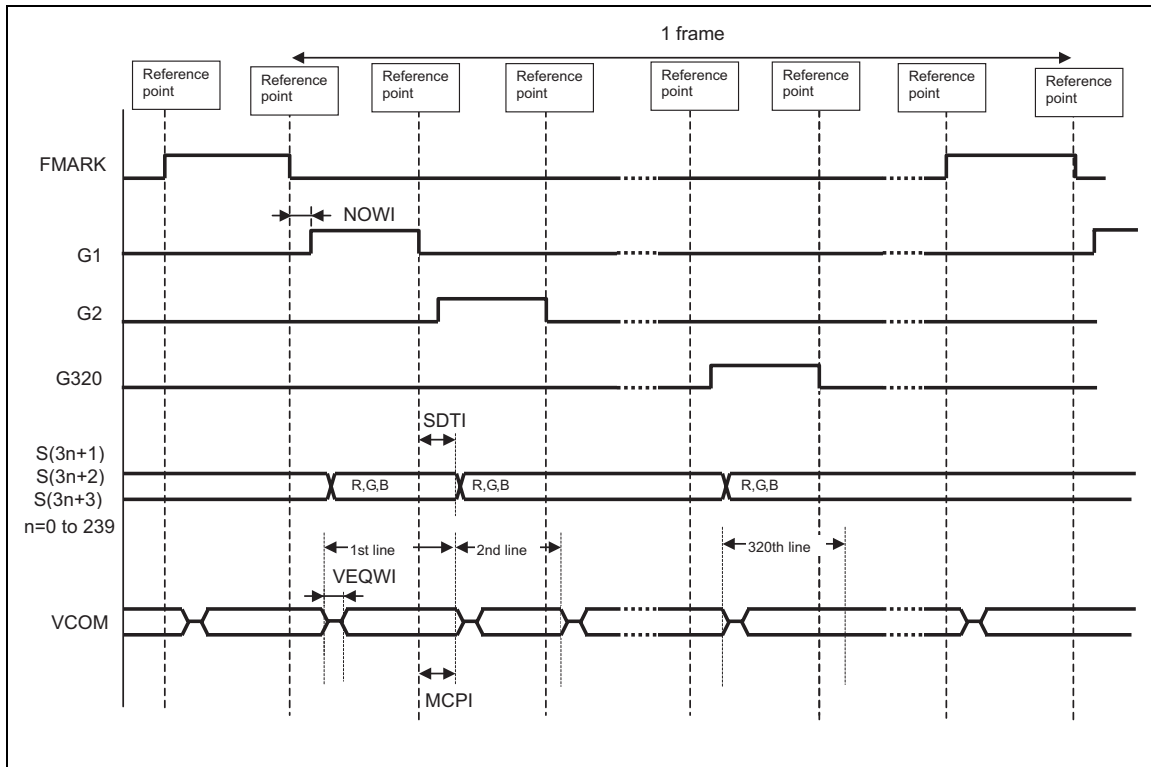


Figure 56

VCOM alternating position and source output alternating position can be set separately.

RGB Interface Operation

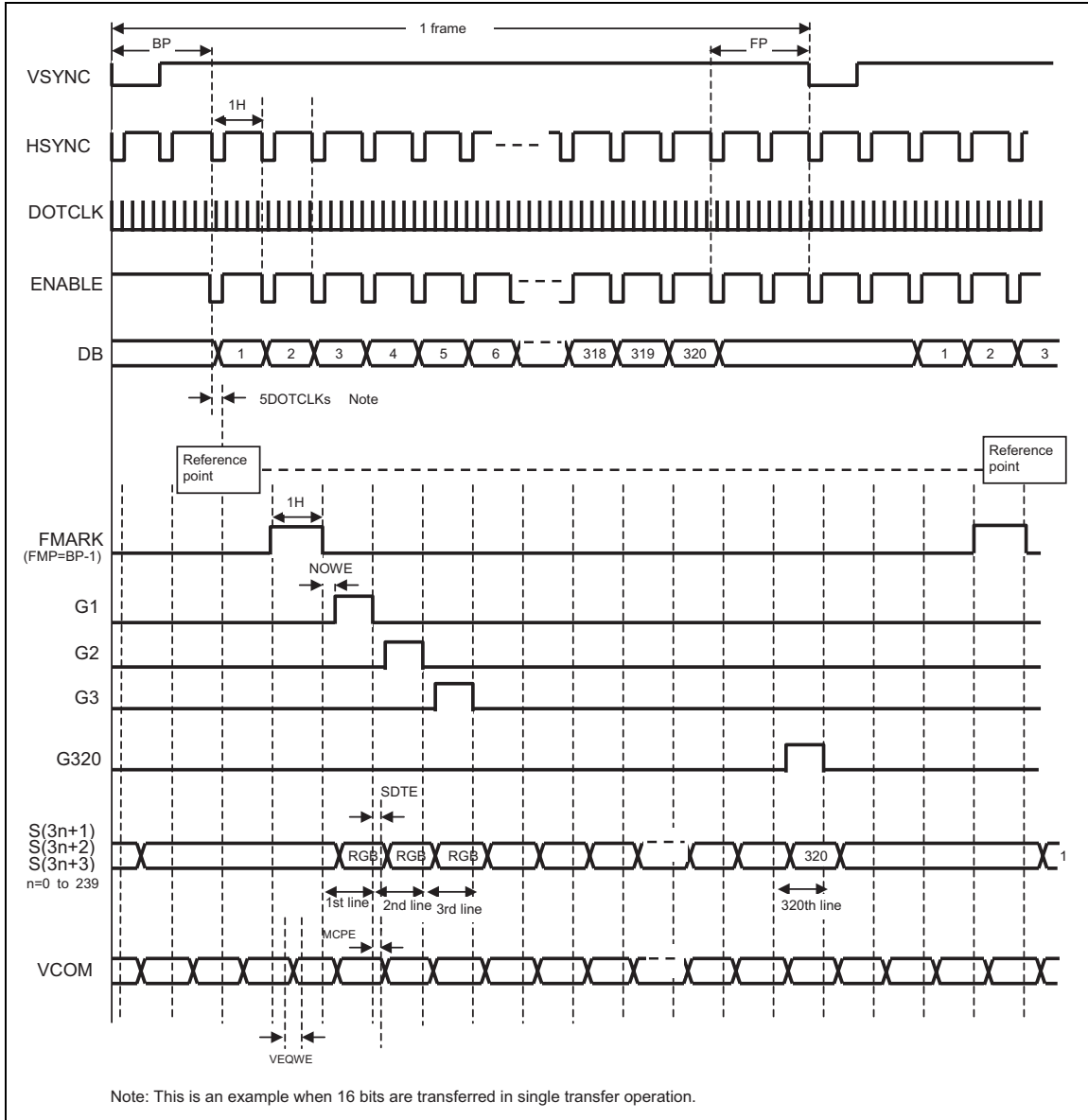


Figure 57

γ Correction Function

γ Correction Function

The R61505W supports γ -correction function to make the optimal colors according to the characteristics of the panel. The R61505W has registers for positive and negative polarities to allow different settings.

γ Correction Circuit

The following figure shows the γ -correction circuit. According to the settings of variable resistors R0 to R8, the voltage level of which is the difference is between VREG1OUT and VGS is evenly divided into 8 grayscale reference voltages (V0, V1, V8, V20, V43, V55, V62 and V63). Other 42-grayscale voltages are generated by setting the level at a certain interval between the reference voltages. For grayscale voltage, see “Grayscale Voltage Calculation Formula”.

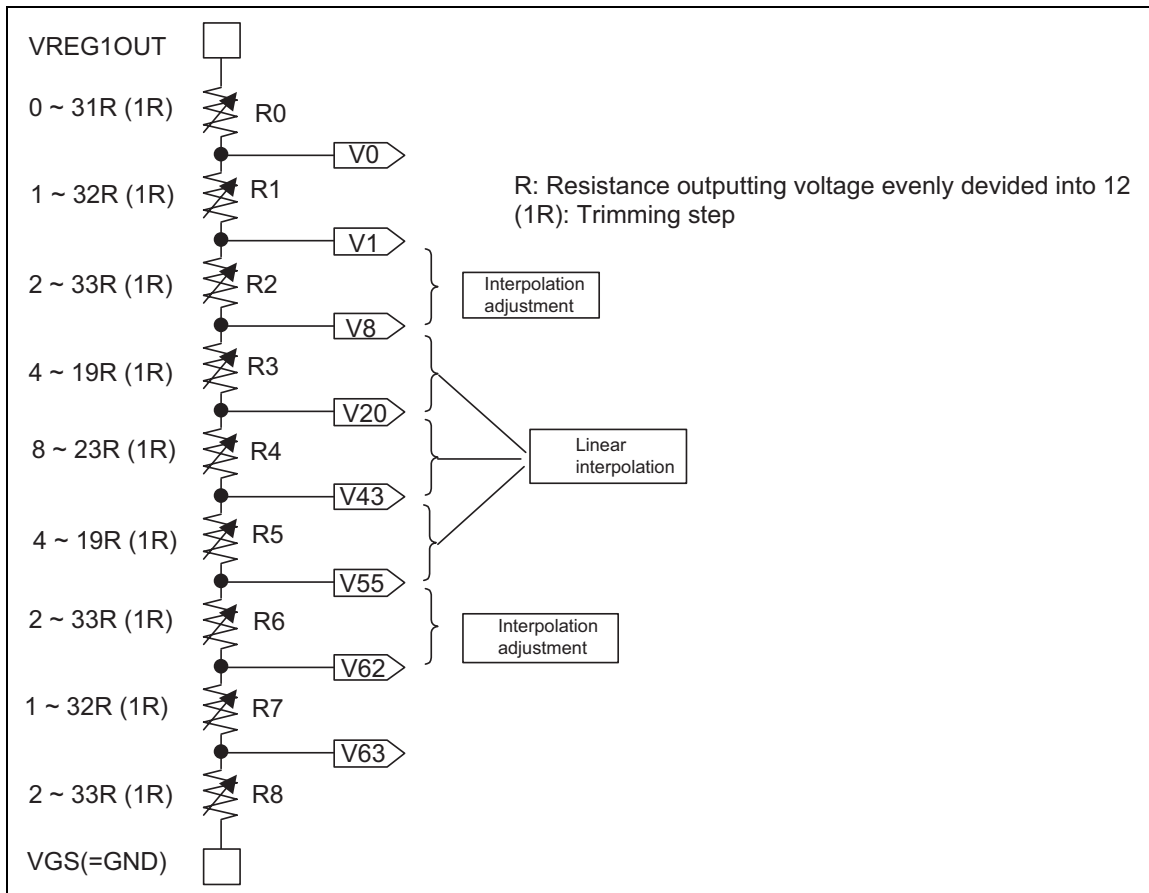


Figure 58

γ Correction Registers

The γ -correction registers include 42-bit reference level adjustment registers for each of positive polarity and negative polarity and 8-bit interpolation adjustment registers.

Reference Level Adjustment Registers**Table 76 Reference Level Adjustment Registers**

| Resistor | Gamma | |
|----------|-------------------|-------------------|
| | Positive polarity | Negative polarity |
| R0 | PR0P00[4:0] | PR0N00[4:0] |
| R1 | PR0P01[4:0] | PR0N01[4:0] |
| R2 | PR0P02[4:0] | PR0N02[4:0] |
| R3 | PR0P03[3:0] | PR0N03[3:0] |
| R4 | PR0P04[3:0] | PR0N04[3:0] |
| R5 | PR0P05[3:0] | PR0N05[3:0] |
| R6 | PR0P06[4:0] | PR0N06[4:0] |
| R7 | PR0P07[4:0] | PR0N07[4:0] |
| R8 | PR0P08[4:0] | PR0N08[4:0] |

Table 77 Reference Level Adjustment Registers and Resistors

| Resistor | Register | | Resistance | Resistor | Register | | Resistance |
|----------|------------|-------|------------|----------|------------|-------|------------|
| | Name | Value | | | Name | Value | |
| R0 | PR**0[4:0] | 5'h00 | 0R | R5 | PR**5[3:0] | 4'h0 | 4R |
| | | 5'h01 | 1R | | | 4'h1 | 5R |
| | | 5'h02 | 2R | | | 4'h2 | 6R |
| | | ⋮ | ⋮ | | | ⋮ | ⋮ |
| | | 5'h1F | 31R | | | 4'hF | 19R |
| R1 | PR**1[4:0] | 5'h00 | 1R | R6 | PR**6[4:0] | 5'h00 | 2R |
| | | 5'h01 | 2R | | | 5'h01 | 3R |
| | | 5'h02 | 3R | | | 5'h02 | 4R |
| | | ⋮ | ⋮ | | | ⋮ | ⋮ |
| | | 5'h1F | 32R | | | 5'h1F | 33R |
| R2 | PR**2[4:0] | 5'h00 | 2R | R7 | PR**7[4:0] | 5'h00 | 1R |
| | | 5'h01 | 3R | | | 5'h01 | 2R |
| | | 5'h02 | 4R | | | 5'h02 | 3R |
| | | ⋮ | ⋮ | | | ⋮ | ⋮ |
| | | 5'h1F | 33R | | | 5'h1F | 32R |
| R3 | PR**3[3:0] | 4'h0 | 4R | R8 | PR**8[4:0] | 5'h00 | 2R |
| | | 4'h1 | 5R | | | 5'h01 | 3R |
| | | 4'h2 | 6R | | | 5'h02 | 4R |
| | | ⋮ | ⋮ | | | ⋮ | ⋮ |
| | | 4'hF | 19R | | | 5'h1F | 33R |
| R4 | PR**4[3:0] | 4'h0 | 8R | | | | |
| | | 4'h1 | 9R | | | | |
| | | 4'h2 | 10R | | | | |
| | | ⋮ | ⋮ | | | | |
| | | 4'hF | 23R | | | | |

Note: ** in the above table represents 0P/0N.

Interpolation Registers

Table 78 Interpolation Registers

| Interpolation adjustment | Gamma | |
|--------------------------|-------------------|-------------------|
| | Positive polarity | Negative polarity |
| V2 ~ V7 | PIOP0[1:0] | PION0[1:0] |
| | PIOP1[1:0] | PION1[1:0] |
| V56 ~ V61 | PIOP2[1:0] | PION2[1:0] |
| | PIOP3[1:0] | PION3[1:0] |

Table 79 Interpolation Factor for V2 to V7

(See “Grayscale Voltage Calculation Formula” for IPV* level)

| PI**0[1:0] | PI**1[1:0] | IPV2 | IPV3 | IPV4 | IPV5 | IPV6 | IPV7 |
|------------|------------|------|------|------|------|------|------|
| 2'h0 | 2'h0 | 81% | 67% | 52% | 39% | 26% | 13% |
| | 2'h1 | 78% | 61% | 43% | 33% | 22% | 11% |
| | 2'h2 | 73% | 52% | 31% | 23% | 15% | 8% |
| | 2'h3 | 72% | 50% | 28% | 21% | 14% | 7% |
| 2'h1 | 2'h0 | 80% | 68% | 56% | 42% | 28% | 14% |
| | 2'h1 | 76% | 62% | 48% | 36% | 24% | 12% |
| | 2'h2 | 70% | 52% | 35% | 26% | 17% | 9% |
| | 2'h3 | 69% | 50% | 31% | 23% | 16% | 8% |
| 2'h2 | 2'h0 | 78% | 70% | 61% | 46% | 30% | 15% |
| | 2'h1 | 74% | 63% | 53% | 39% | 26% | 13% |
| | 2'h2 | 66% | 53% | 39% | 29% | 20% | 10% |
| | 2'h3 | 64% | 50% | 36% | 27% | 18% | 9% |
| 2'h3 | 2'h0 | 78% | 70% | 63% | 47% | 31% | 16% |
| | 2'h1 | 73% | 64% | 54% | 41% | 27% | 14% |
| | 2'h2 | 65% | 53% | 41% | 31% | 20% | 10% |
| | 2'h3 | 63% | 50% | 37% | 28% | 19% | 9% |

Table 80 Interpolation Factor for V56 to V61

| PI**3[1:0] | PI**2[1:0] | IPV56 | IPV57 | IPV58 | IPV59 | IPV60 | IPV61 |
|------------|------------|-------|-------|-------|-------|-------|-------|
| 2'h0 | 2'h0 | 87% | 74% | 61% | 48% | 33% | 19% |
| | 2'h1 | 89% | 78% | 67% | 57% | 39% | 22% |
| | 2'h2 | 92% | 85% | 77% | 69% | 48% | 27% |
| | 2'h3 | 93% | 86% | 79% | 72% | 50% | 28% |
| 2'h1 | 2'h0 | 86% | 72% | 58% | 44% | 32% | 20% |
| | 2'h1 | 88% | 76% | 64% | 52% | 38% | 24% |
| | 2'h2 | 91% | 83% | 74% | 65% | 48% | 30% |
| | 2'h3 | 92% | 84% | 77% | 69% | 50% | 31% |
| 2'h2 | 2'h0 | 85% | 70% | 54% | 39% | 30% | 22% |
| | 2'h1 | 87% | 74% | 61% | 47% | 37% | 26% |
| | 2'h2 | 90% | 80% | 71% | 61% | 47% | 34% |
| | 2'h3 | 91% | 82% | 73% | 64% | 50% | 36% |
| 2'h3 | 2'h0 | 84% | 69% | 53% | 38% | 30% | 22% |
| | 2'h1 | 86% | 73% | 59% | 46% | 36% | 27% |
| | 2'h2 | 90% | 80% | 69% | 59% | 47% | 35% |
| | 2'h3 | 91% | 81% | 72% | 63% | 50% | 37% |

Note: ** in the above tables represents 0P/0N.

Table 81 Grayscale Voltage Calculation Formula

| Grayscale voltage | Formula | Grayscale voltage | Formula |
|-------------------|---|-------------------|---|
| V0 | $\Delta V \times \Sigma (R1 \sim R8) / \text{SUMR}$ | V32 | $V43 + (V20 - V43) \times 11/23$ |
| V1 | $\Delta V \times \Sigma (R2 \sim R8) / \text{SUMR}$ | V33 | $V43 + (V20 - V43) \times 10/23$ |
| V2 | $V8 + (V1 - V8) \times \text{IPV2}$ | V34 | $V43 + (V20 - V43) \times 9/23$ |
| V3 | $V8 + (V1 - V8) \times \text{IPV3}$ | V35 | $V43 + (V20 - V43) \times 8/23$ |
| V4 | $V8 + (V1 - V8) \times \text{IPV4}$ | V36 | $V43 + (V20 - V43) \times 7/23$ |
| V5 | $V8 + (V1 - V8) \times \text{IPV5}$ | V37 | $V43 + (V20 - V43) \times 6/23$ |
| V6 | $V8 + (V1 - V8) \times \text{IPV6}$ | V38 | $V43 + (V20 - V43) \times 5/23$ |
| V7 | $V8 + (V1 - V8) \times \text{IPV7}$ | V39 | $V43 + (V20 - V43) \times 4/23$ |
| V8 | $\Delta V \times \Sigma (R3 \sim R8) / \text{SUMR}$ | V40 | $V43 + (V20 - V43) \times 3/23$ |
| V9 | $V20 + (V8 - V20) \times 11/12$ | V41 | $V43 + (V20 - V43) \times 2/23$ |
| V10 | $V20 + (V8 - V20) \times 10/12$ | V42 | $V43 + (V20 - V43) \times 1/23$ |
| V11 | $V20 + (V8 - V20) \times 9/12$ | V43 | $\Delta V \times \Sigma (R5 \sim R8) / \text{SUMR}$ |
| V12 | $V20 + (V8 - V20) \times 8/12$ | V44 | $V55 + (V43 - V55) \times 11/12$ |
| V13 | $V20 + (V8 - V20) \times 7/12$ | V45 | $V55 + (V43 - V55) \times 10/12$ |
| V14 | $V20 + (V8 - V20) \times 6/12$ | V46 | $V55 + (V43 - V55) \times 9/12$ |
| V15 | $V20 + (V8 - V20) \times 5/12$ | V47 | $V55 + (V43 - V55) \times 8/12$ |
| V16 | $V20 + (V8 - V20) \times 4/12$ | V48 | $V55 + (V43 - V55) \times 7/12$ |
| V17 | $V20 + (V8 - V20) \times 3/12$ | V49 | $V55 + (V43 - V55) \times 6/12$ |
| V18 | $V20 + (V8 - V20) \times 2/12$ | V50 | $V55 + (V43 - V55) \times 5/12$ |
| V19 | $V20 + (V8 - V20) \times 1/12$ | V51 | $V55 + (V43 - V55) \times 4/12$ |
| V20 | $\Delta V \times \Sigma (R4 \sim R8) / \text{SUMR}$ | V52 | $V55 + (V43 - V55) \times 3/12$ |
| V21 | $V43 + (V20 - V43) \times 22/23$ | V53 | $V55 + (V43 - V55) \times 2/12$ |
| V22 | $V43 + (V20 - V43) \times 21/23$ | V54 | $V55 + (V43 - V55) \times 1/12$ |
| V23 | $V43 + (V20 - V43) \times 20/23$ | V55 | $\Delta V \times \Sigma (R6 \sim R8) / \text{SUMR}$ |
| V24 | $V43 + (V20 - V43) \times 19/23$ | V56 | $V62 + (V55 - V62) \times \text{IPV56}$ |
| V25 | $V43 + (V20 - V43) \times 18/23$ | V57 | $V62 + (V55 - V62) \times \text{IPV57}$ |
| V26 | $V43 + (V20 - V43) \times 17/23$ | V58 | $V62 + (V55 - V62) \times \text{IPV58}$ |
| V27 | $V43 + (V20 - V43) \times 16/23$ | V59 | $V62 + (V55 - V62) \times \text{IPV59}$ |
| V28 | $V43 + (V20 - V43) \times 15/23$ | V60 | $V62 + (V55 - V62) \times \text{IPV60}$ |
| V29 | $V43 + (V20 - V43) \times 14/23$ | V61 | $V62 + (V55 - V62) \times \text{IPV61}$ |
| V30 | $V43 + (V20 - V43) \times 13/23$ | V62 | $\Delta V \times (R7 + R8) / \text{SUMR}$ |
| V31 | $V43 + (V20 - V43) \times 12/23$ | V63 | $\Delta V \times R8 / \text{SUMR}$ |

Note: Make sure that
 $\Delta V = V_{\text{REG1OUT}} - V_{\text{GS}}$
 $\text{SUMR} = \Sigma(R0 \sim R8) \geq 70R$
 $V63 \geq 0.2V$

Table 82 Frame Memory Data and the Grayscale Voltage

| Frame Memory data | Grayscale voltage | | | | Frame memory data | Grayscale voltage | | | |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| | REV = 1 | | REV = 0 | | | REV = 1 | | REV = 0 | |
| | Positive polarity | Negative polarity | Positive polarity | Negative polarity | | Positive polarity | Negative polarity | Positive polarity | Negative polarity |
| 6'h00 | V0 | V63 | V63 | V0 | 6'h20 | V32 | V31 | V31 | V32 |
| 6'h01 | V1 | V62 | V62 | V1 | 6'h21 | V33 | V30 | V30 | V33 |
| 6'h02 | V2 | V61 | V61 | V2 | 6'h22 | V34 | V29 | V29 | V34 |
| 6'h03 | V3 | V60 | V60 | V3 | 6'h23 | V35 | V28 | V28 | V35 |
| 6'h04 | V4 | V59 | V59 | V4 | 6'h24 | V36 | V27 | V27 | V36 |
| 6'h05 | V5 | V58 | V58 | V5 | 6'h25 | V37 | V26 | V26 | V37 |
| 6'h06 | V6 | V57 | V57 | V6 | 6'h26 | V38 | V25 | V25 | V38 |
| 6'h07 | V7 | V56 | V56 | V7 | 6'h27 | V39 | V24 | V24 | V39 |
| 6'h08 | V8 | V55 | V55 | V8 | 6'h28 | V40 | V23 | V23 | V40 |
| 6'h09 | V9 | V54 | V54 | V9 | 6'h29 | V41 | V22 | V22 | V41 |
| 6'h0A | V10 | V53 | V53 | V10 | 6'h2A | V42 | V21 | V21 | V42 |
| 6'h0B | V11 | V52 | V52 | V11 | 6'h2B | V43 | V20 | V20 | V43 |
| 6'h0C | V12 | V51 | V51 | V12 | 6'h2C | V44 | V19 | V19 | V44 |
| 6'h0D | V13 | V50 | V50 | V13 | 6'h2D | V45 | V18 | V18 | V45 |
| 6'h0E | V14 | V49 | V49 | V14 | 6'h2E | V46 | V17 | V17 | V46 |
| 6'h0F | V15 | V48 | V48 | V15 | 6'h2F | V47 | V16 | V16 | V47 |
| 6'h10 | V16 | V47 | V47 | V16 | 6'h30 | V48 | V15 | V15 | V48 |
| 6'h11 | V17 | V46 | V46 | V17 | 6'h31 | V49 | V14 | V14 | V49 |
| 6'h12 | V18 | V45 | V45 | V18 | 6'h32 | V50 | V13 | V13 | V50 |
| 6'h13 | V19 | V44 | V44 | V19 | 6'h33 | V51 | V12 | V12 | V51 |
| 6'h14 | V20 | V43 | V43 | V20 | 6'h34 | V52 | V11 | V11 | V52 |
| 6'h15 | V21 | V42 | V42 | V21 | 6'h35 | V53 | V10 | V10 | V53 |
| 6'h16 | V22 | V41 | V41 | V22 | 6'h36 | V54 | V9 | V9 | V54 |
| 6'h17 | V23 | V40 | V40 | V23 | 6'h37 | V55 | V8 | V8 | V55 |
| 6'h18 | V24 | V39 | V39 | V24 | 6'h38 | V56 | V7 | V7 | V56 |
| 6'h19 | V25 | V38 | V38 | V25 | 6'h39 | V57 | V6 | V6 | V57 |
| 6'h1A | V26 | V37 | V37 | V26 | 6'h3A | V58 | V5 | V5 | V58 |
| 6'h1B | V27 | V36 | V36 | V27 | 6'h3B | V59 | V4 | V4 | V59 |
| 6'h1C | V28 | V35 | V35 | V28 | 6'h3C | V60 | V3 | V3 | V60 |
| 6'h1D | V29 | V34 | V34 | V29 | 6'h3D | V61 | V2 | V2 | V61 |
| 6'h1E | V30 | V33 | V33 | V30 | 6'h3E | V62 | V1 | V1 | V62 |
| 6'h1F | V31 | V32 | V32 | V31 | 6'h3F | V63 | V0 | V0 | V63 |

Power Supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the R61505W.

Power Supply Circuit Connection Example 1

VCI1 voltage level is defined by VC bit (R11h).

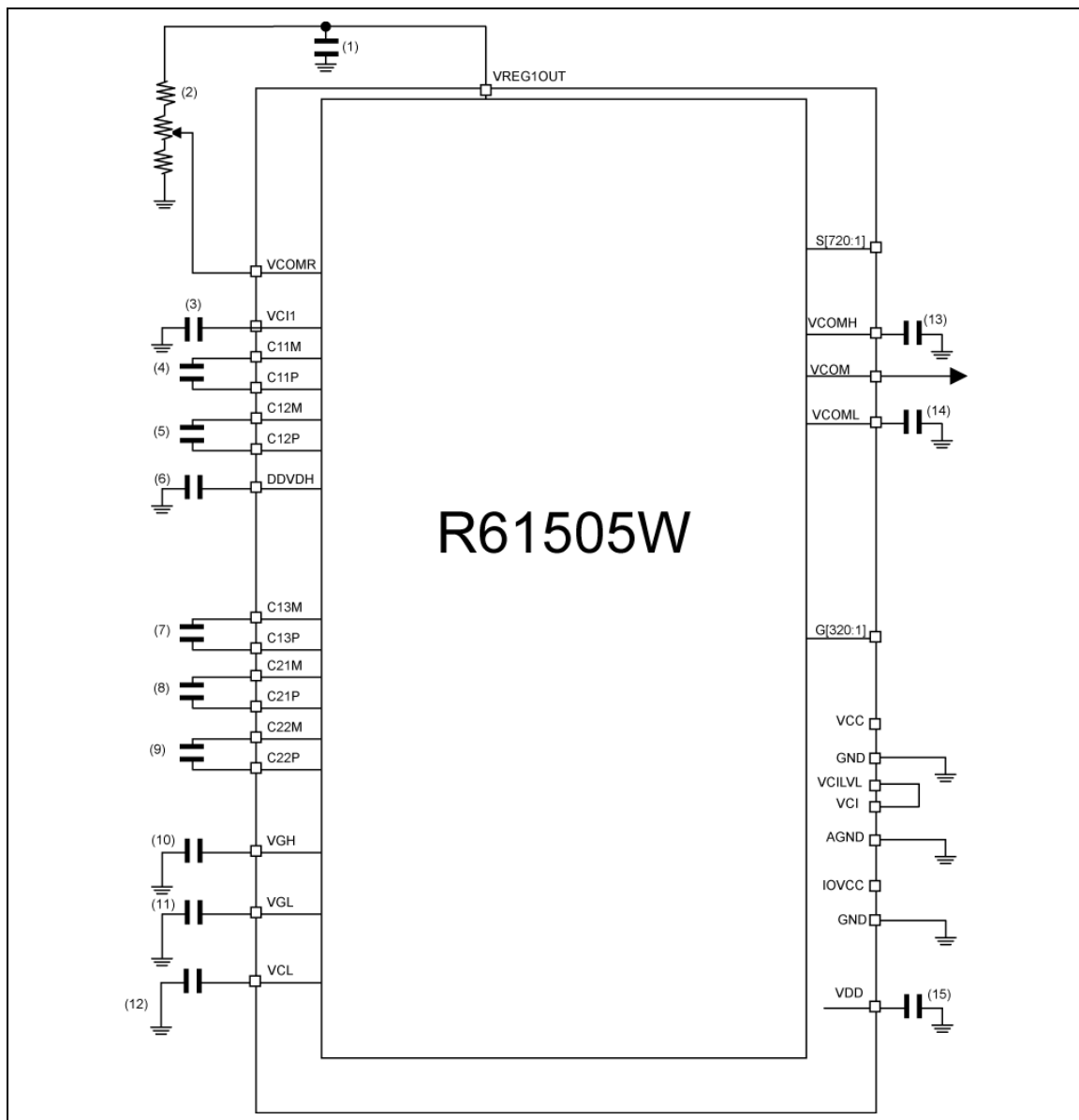


Figure 59

Power Supply Circuit Connection Example 2 (VCI voltage is directly applied to VCI1 pin)

In the following example, the electrical potential VCI is directly applied to VCI1. In this case, step-up operation is more effective although VCI1 voltage level cannot be defined by VC bit (R11h).

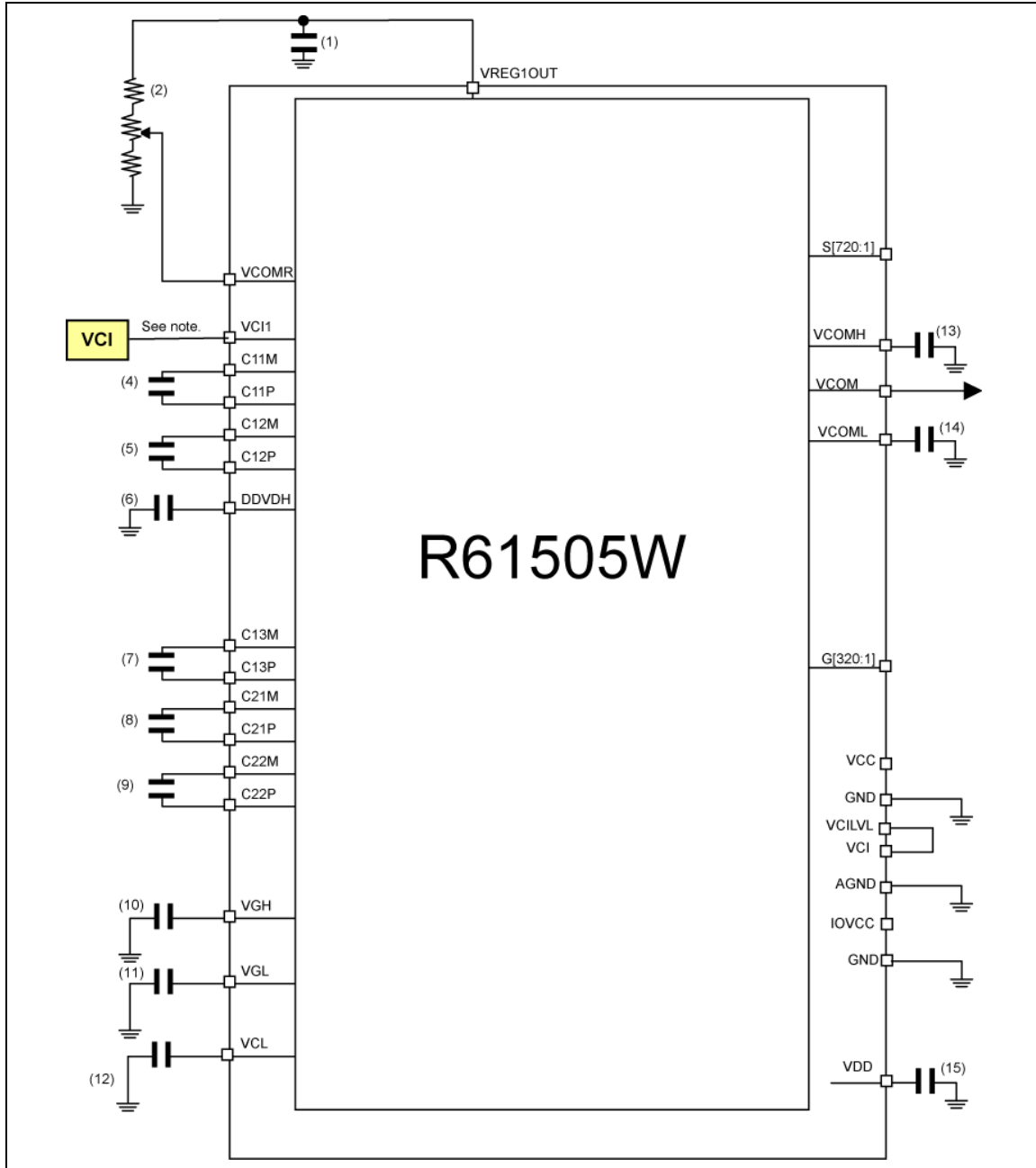


Figure 60

Note: When directly applying the VCI level to VCI1, set VC = 3'h7. Capacitor connection to VCIOUT is not required.

Specifications of Power Supply Circuit External Elements

The specifications of external elements connected to the power supply circuit of the R61505W are as follows. The numbers in the parentheses correspond with the numbers of the elements in the section "Power Supply Generating Circuit".

Table 83 Capacitor

| Capacitance | Voltage proof | Pin Connection |
|----------------------------------|---------------|---|
| 1 μ F (B characteristics) | 6V | (1) VREG1OUT, (3) VCI1, (4) C11P, C11M, (5) C12P, C12M, (7) C13P, C13M, (12) VCL, (13) VCOMH, (14) VCOML |
| | 3V | (15) VDD |
| | 10V | (6) DDVDH, (8) C21P, C21M, (9) C22P, C22M |
| | 25V | (10) VGH, (11) VGL |

Table 84 Variable Resistor

| Specification | Pin Connection |
|------------------|----------------|
| > 200 k Ω | (2) VCOMR |

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61505W and the TFT display application voltage waveforms and electrical potential relationship.

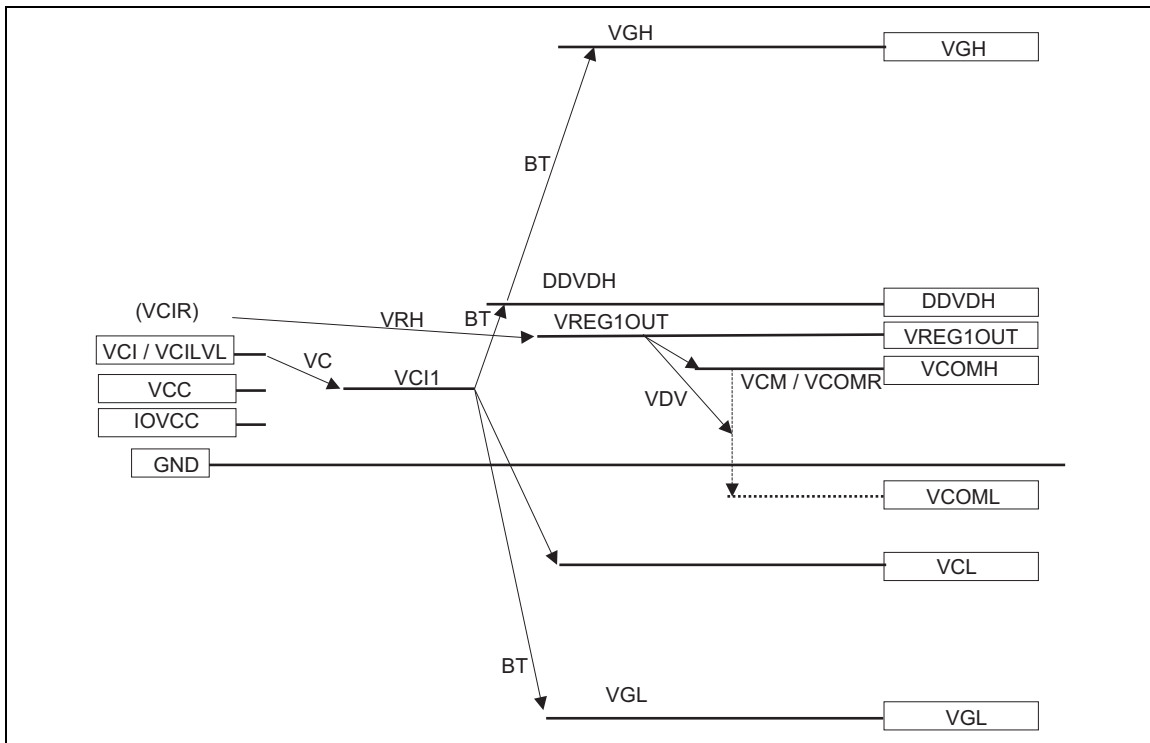


Figure 61

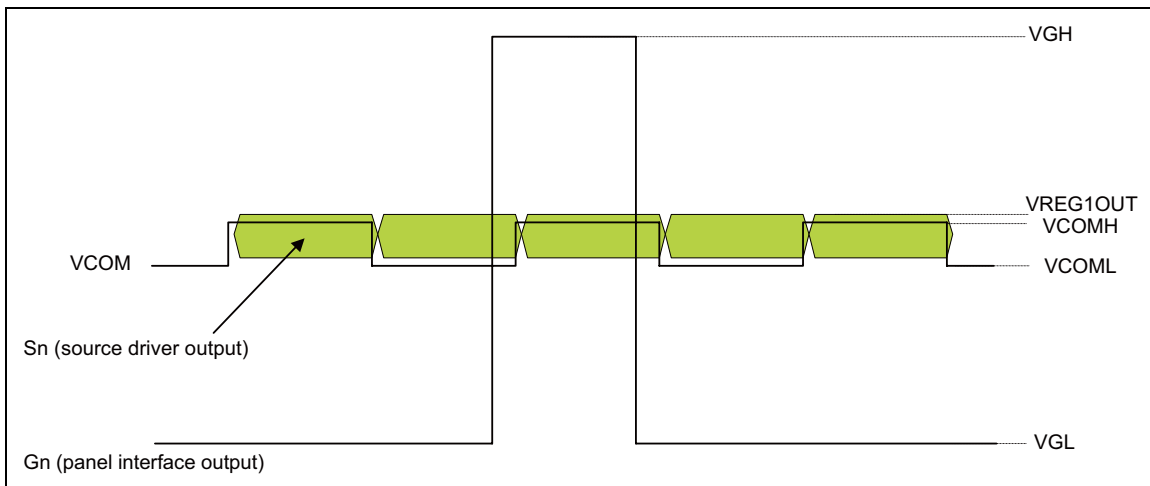


Figure 62 Liquid Crystal Application Voltage Waveform and Electrical Potential

VCOMH Voltage Adjustment Sequence

When adjusting the VCOMH voltage by setting VCM1 [6:0] in the R29'h register (internal VCOMH level adjustment circuit), follow the sequence below. The R61505W can retain the VCOMH level adjustment setting values in NVM, which allows erasing 5 times.

To write data onto the NVM, set VCOMH adjusting register VCM1 [6:0] (R29h), VCMSEL and VCM2[6:0] (R2Ah) so that these registers correspond with NVM write data register NVDAT [15:0]. See NVM write, read and erase sequences in the section "NVM Control Sequence".

If data has been erased from the bit, the bit value is set to "1". The bit to which data is not written should be set to 1.

If VCMSEL=1, VCM1 is enabled. If VCMSEL=0, VCM2 is enabled.

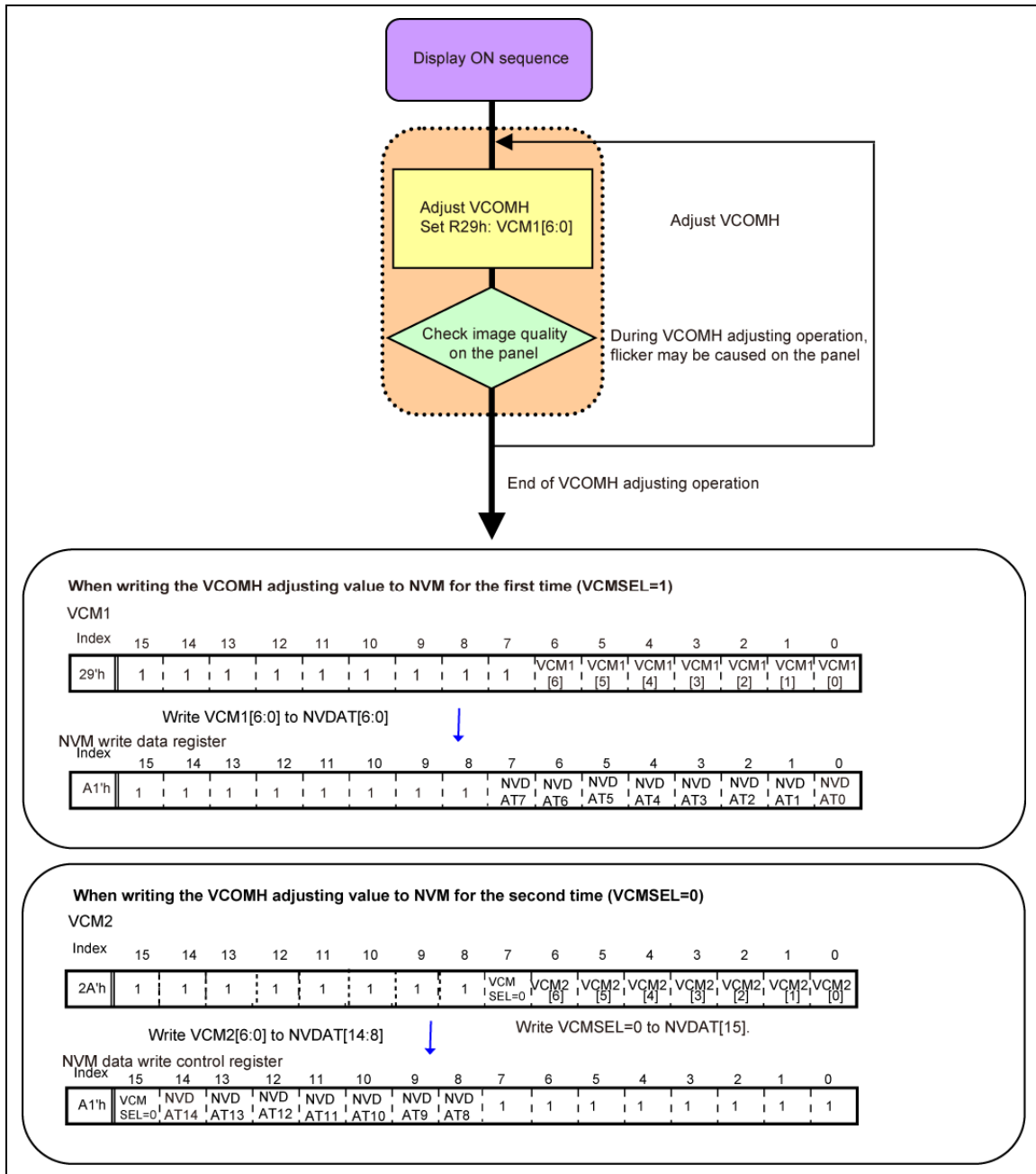


Figure 63

NVM Control Sequence

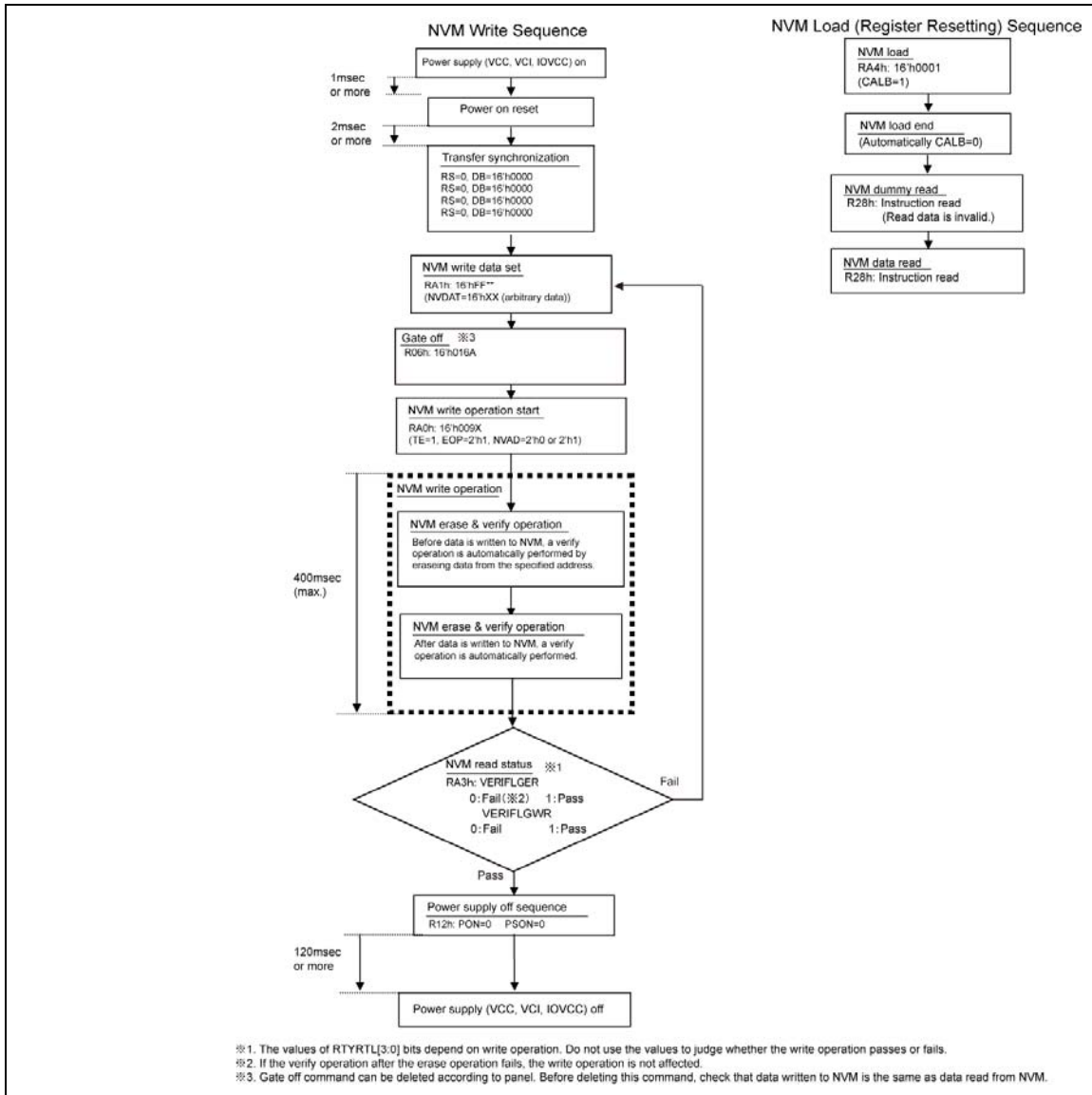


Figure 64

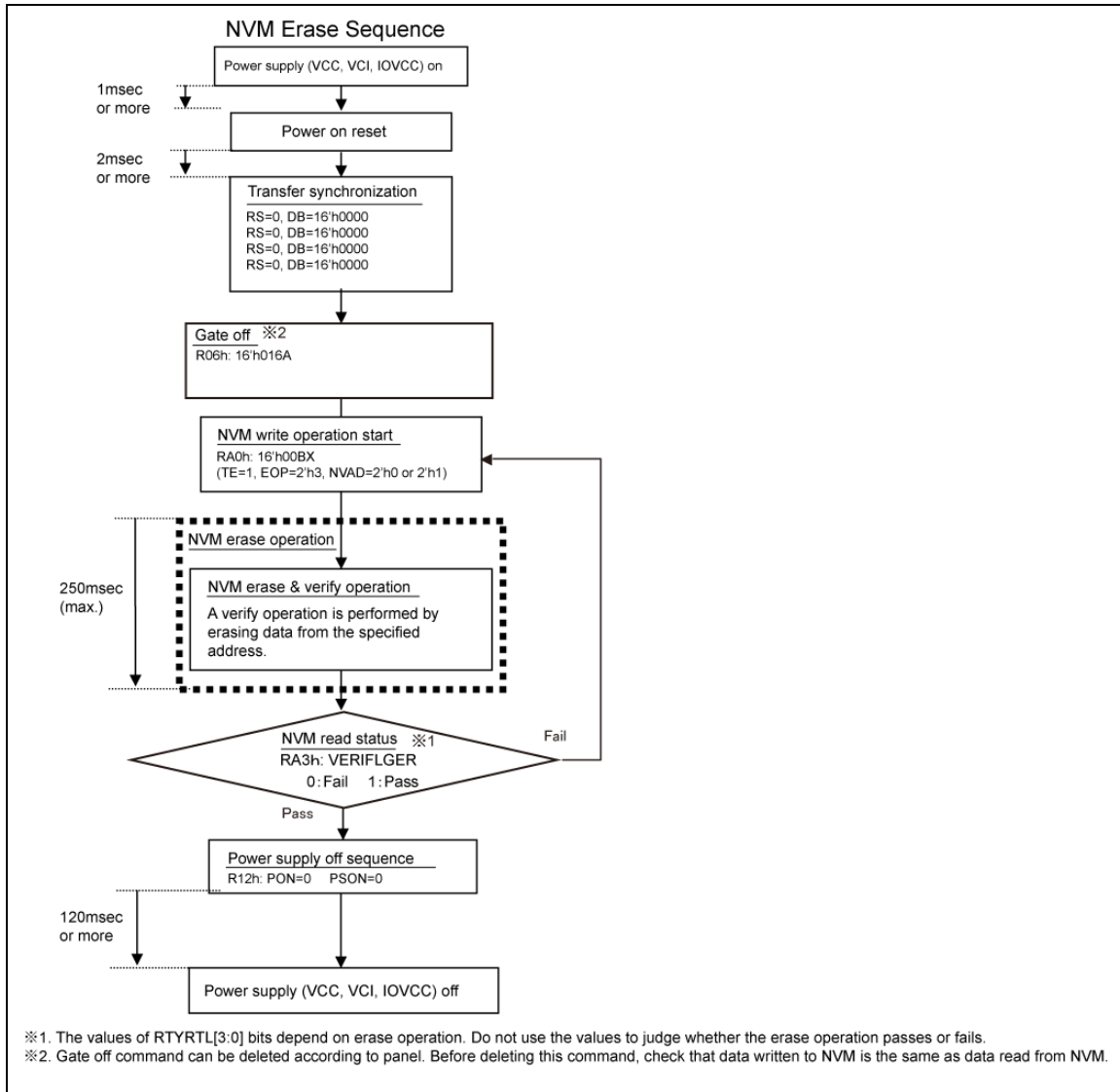


Figure 65

Power Supply Setting Sequence

R61505W Setting Sequence

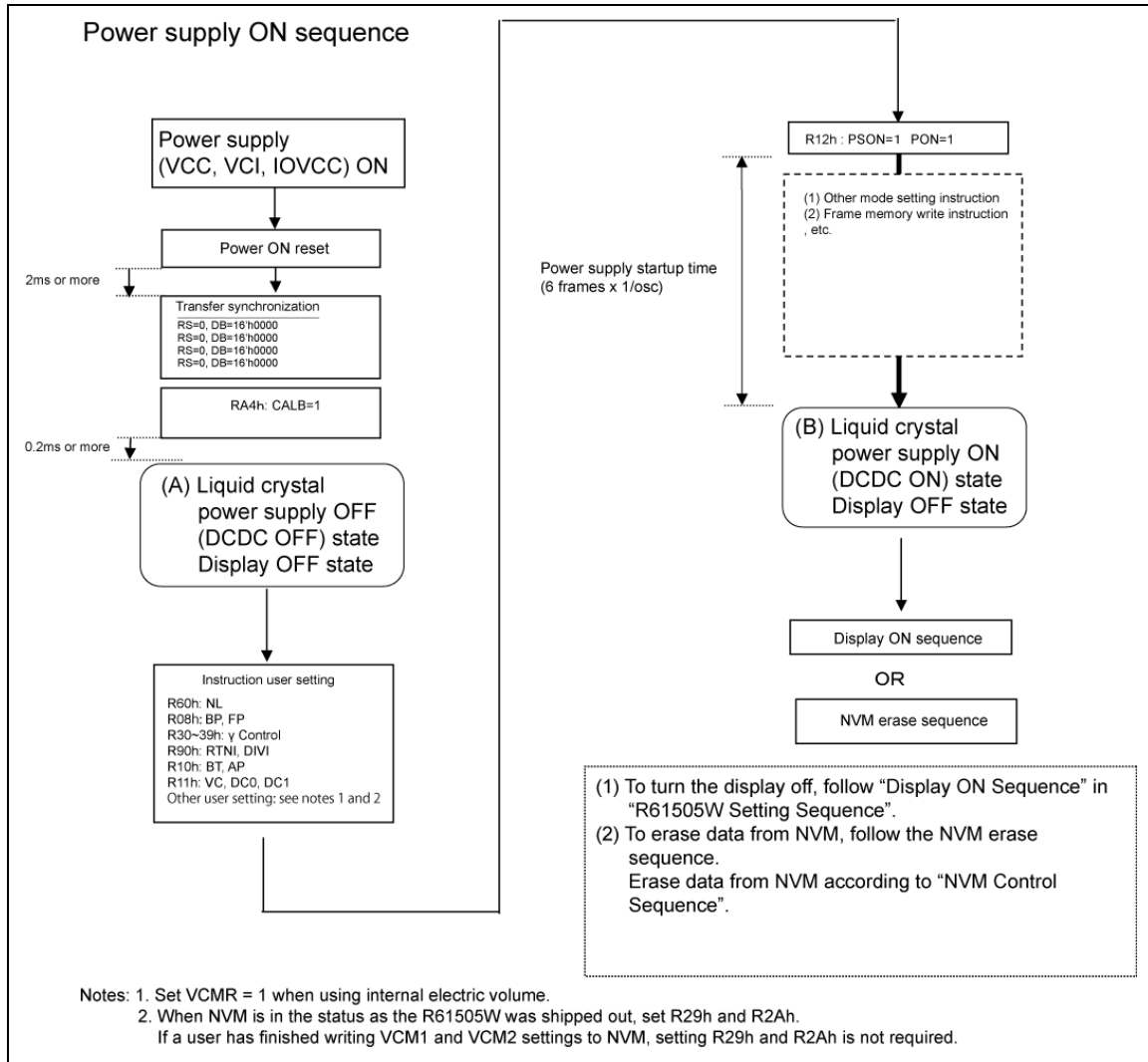
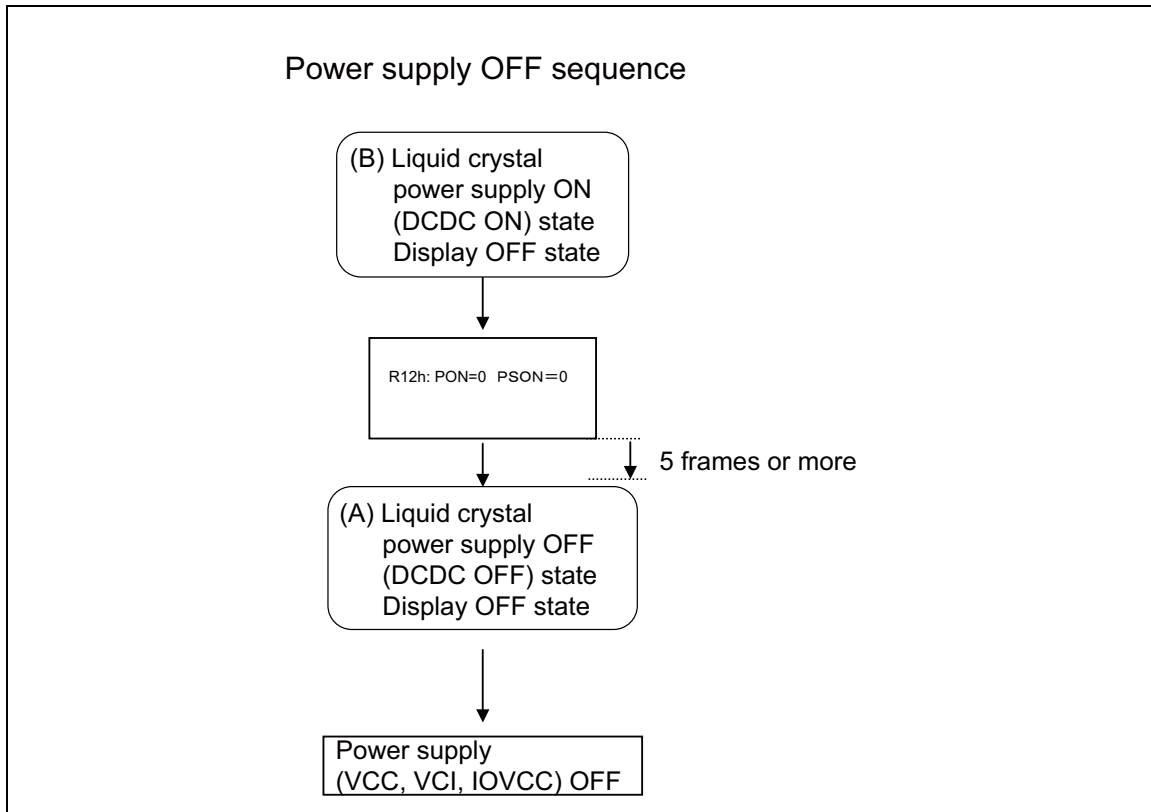


Figure 66

**Figure 67**

Instruction Setting Sequence

R61505W Setting Sequence

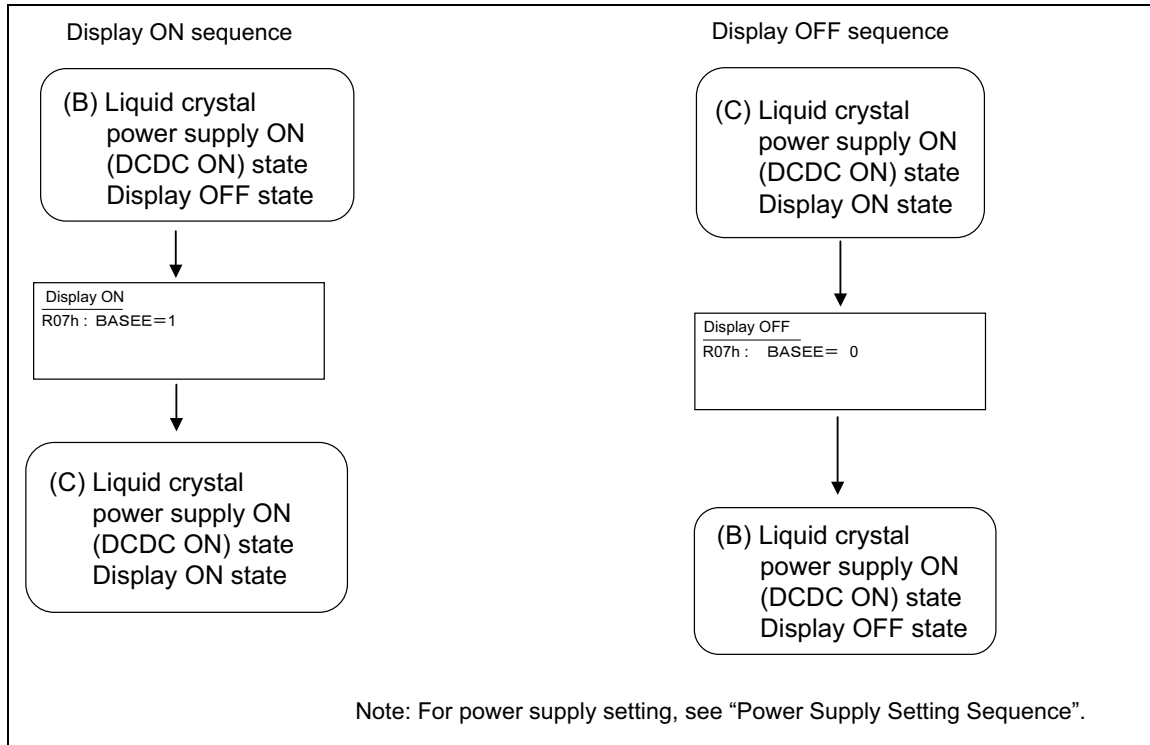


Figure 68

Other Mode Transition Setting Sequences

Deep Standby Mode IN/EXIT Sequences

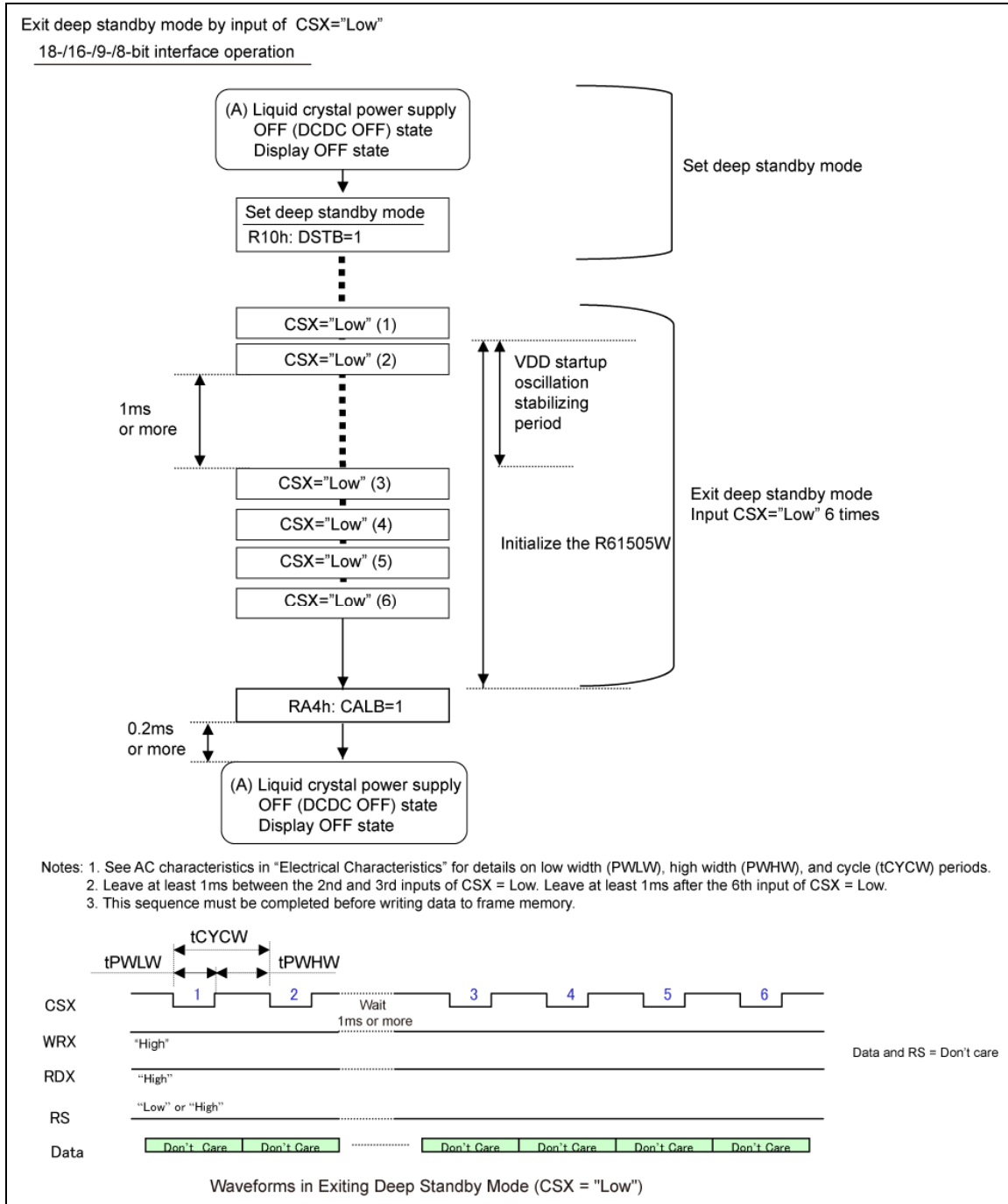


Figure 69 Exit Deep Standby Mode by Input of CSX ="Low" (18-/ 16-/ 9-/ 8-Bit Interface)

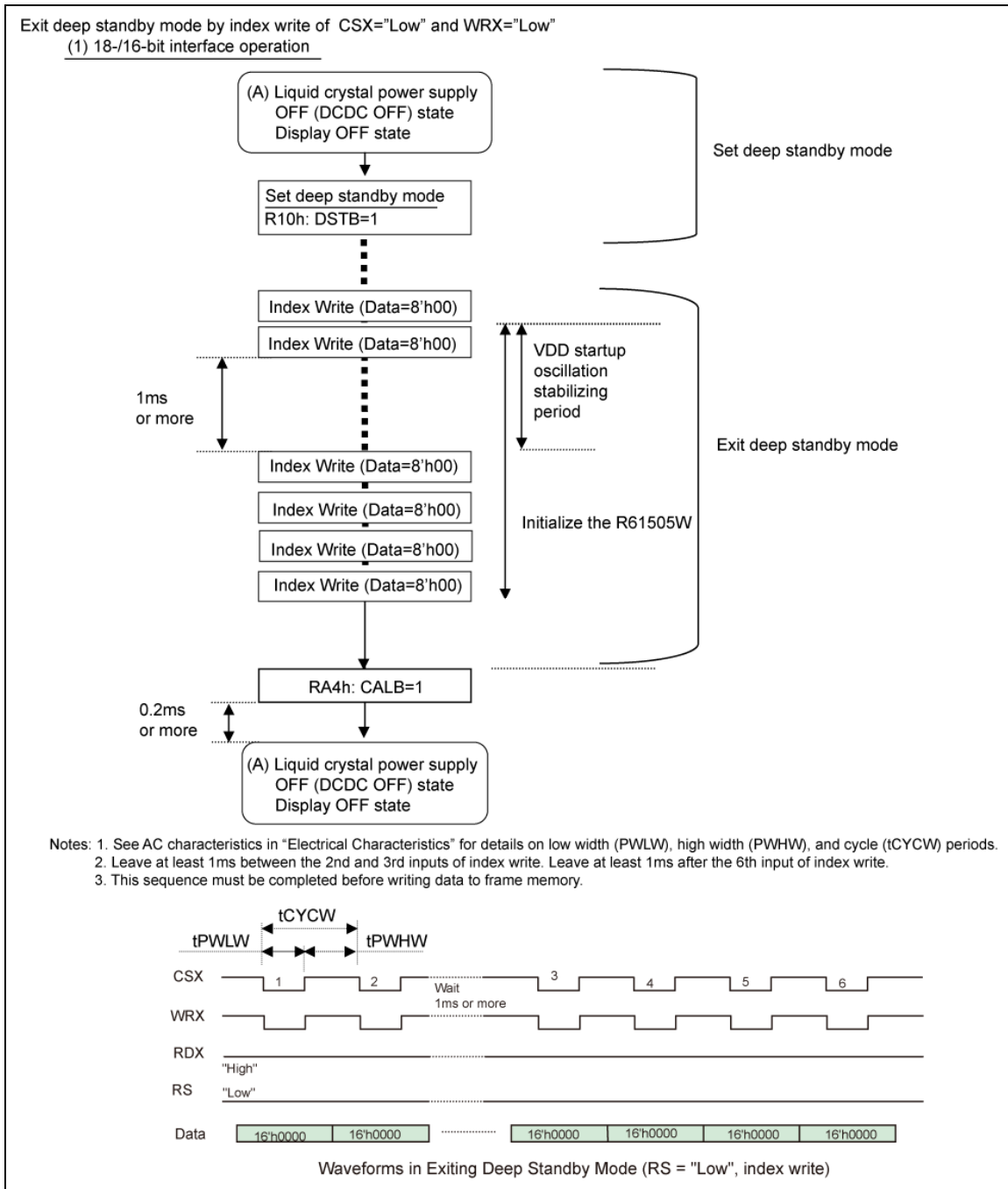


Figure 70 Exit Deep Standby Mode by Index Write of CSX="Low" and WRX="Low" (18-/16-Bit Interface Operation)

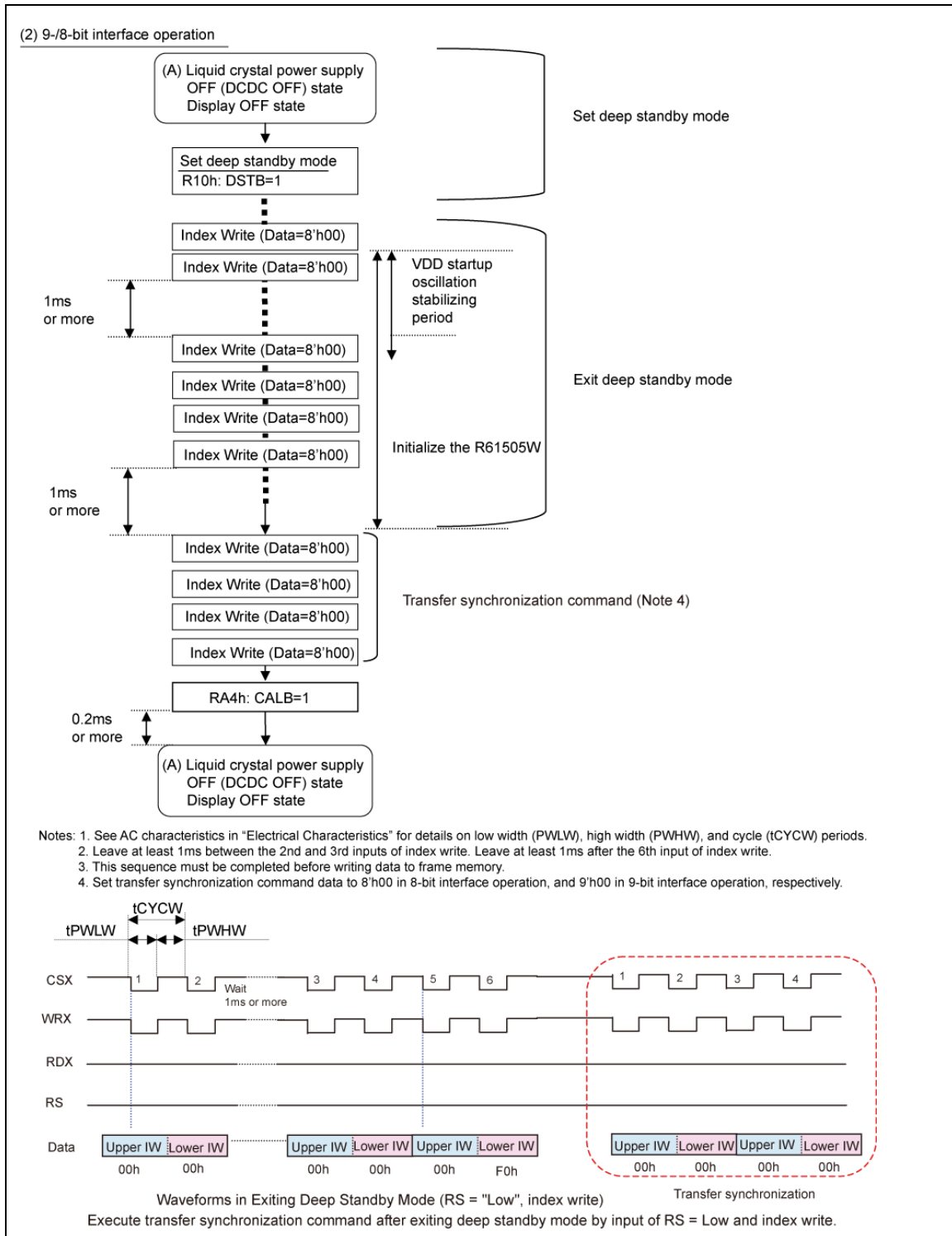


Figure 71 Exit Deep Standby Mode by Index Write of CSX="Low" and WRX="Low" (9-/8-Bit Interface Operation)

8-Color Mode Setting

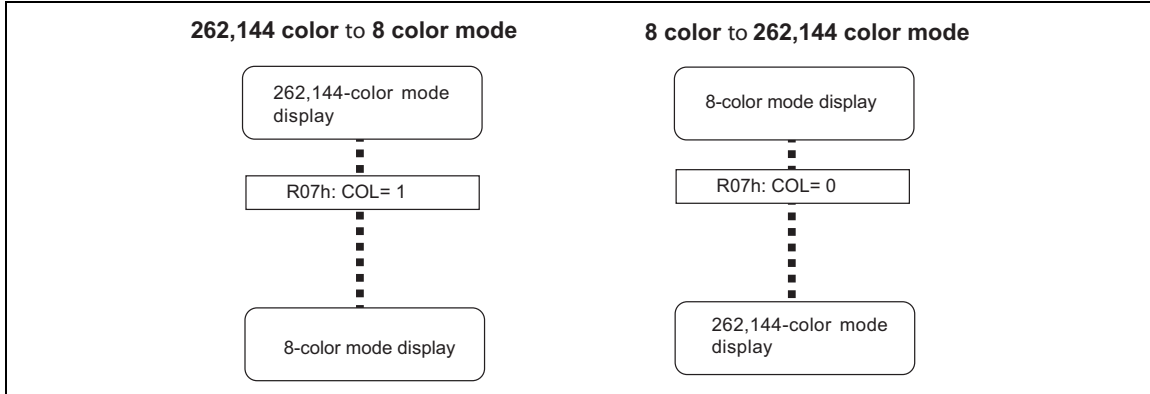


Figure 72

Partial Display Setting

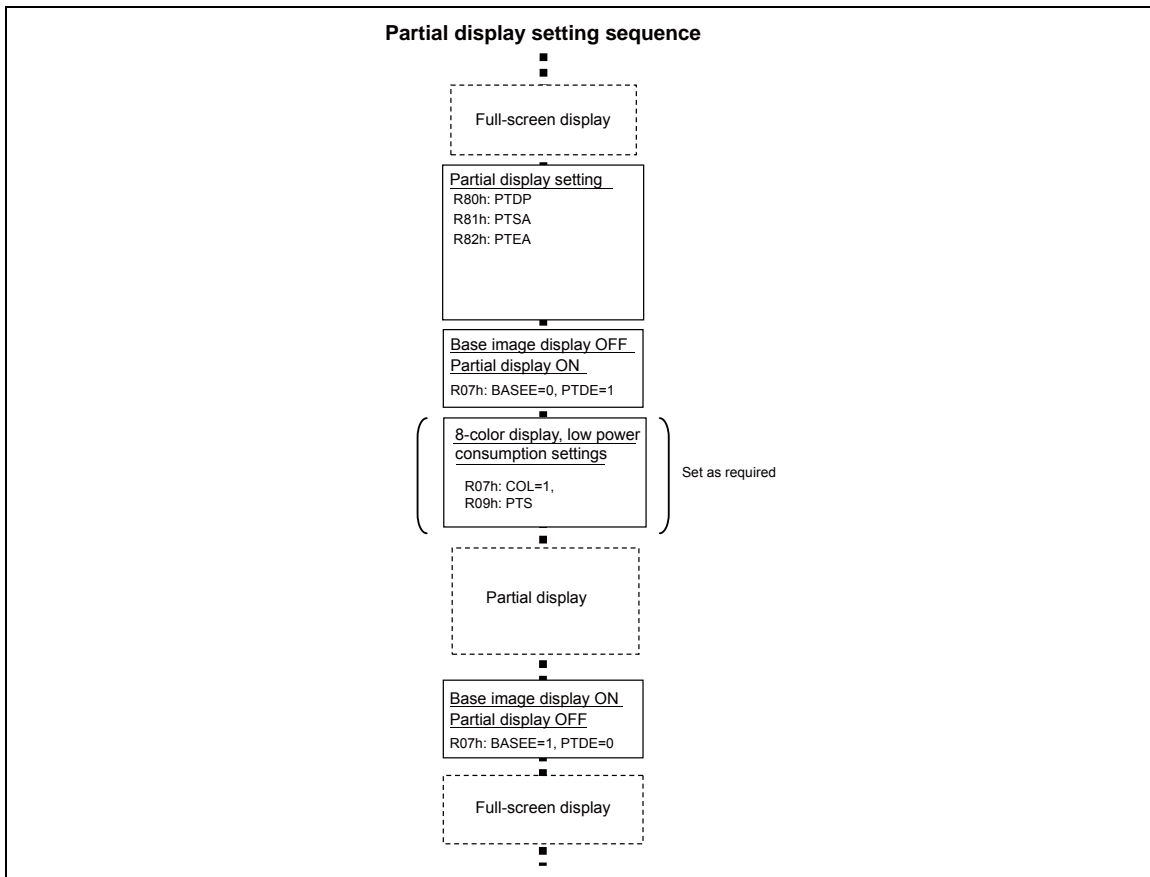


Figure 73

Absolute Maximum Ratings

Table 85

| Item | Symbol | Unit | Value | Note |
|------------------------|--------------|------|--------------------|------|
| Power Supply Voltage 1 | VCC, IOVCC | V | -0.3 ~ +4.6 | 1, 2 |
| Power Supply Voltage 2 | VCI – AGND | V | -0.3 ~ +4.6 | 1, 3 |
| Power Supply Voltage 3 | DDVDH – AGND | V | -0.3 ~ +6.5 | 1, 4 |
| Power Supply Voltage 4 | AGND – VCL | V | -0.3 ~ +4.6 | 1 |
| Power Supply Voltage 5 | DDVDH – VCL | V | -0.3 ~ +9.0 | 1, 5 |
| Power Supply Voltage 7 | AGND – VGL | V | -0.3 ~ +13.0 | 1, 6 |
| Power Supply Voltage 8 | VGH– VGL | V | -0.3 ~ +30.0 | 1 |
| Input Voltage | Vt | V | -0.3 ~ IOVCC + 0.3 | 1 |
| Operating Temperature | Topr | °C | -40 ~ +85 | 1, 7 |
| NVM Write Temperature | Twep | °C | +20 ~ +30 | 1 |
| NVM Erase Temperature | Teep | °C | +20 ~ +30 | 1 |
| Storage Temperature | Tstg | °C | -55 ~ +110 | 1 |

Notes: 1. If the R61505W is used beyond the absolute maximum ratings, the LSI may be permanently damaged. It is strongly recommended to use the LSI under the condition within the electrical characteristics in normal operation. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

2. Make sure VCC (high) \geq GND (low), IOVCC (high) \geq GND (low).
3. Make sure VCI (high) \geq AGND (low).
4. Make sure DDVDH (high) \geq AGND (low).
5. Make sure DDVDH (high) \geq VCL (low).
6. Make sure AGND (high) \geq VGL (low).
7. The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Electrical Characteristics

DC Characteristics 1

Table 86 (VCC= 2.50V~3.30V, IOVCC=1.65V~3.30V, Ta=-40C~+85C) (See note 1)

| Item | Symbol | Unit | Test Condition | Min. | Typ. | Max. | Note |
|---|-------------------|------|--|-----------------|------|-----------------|------|
| Input "High" level voltage 1 Except RESETX pin | V _{IH1} | V | IOVCC=1.65V ~ 3.30V | 0.80 × IOVCC | — | IOVCC | 2, 3 |
| Input "Low" level voltage 1 Except RESETX pin | V _{IL1} | V | IOVCC=1.65V ~ 3.30V | -0.3 | — | 0.20 × IOVCC | 2, 3 |
| Input "High" level voltage 2 RESETX pin | V _{IH2} | V | IOVCC=1.65V ~ 3.30V | 0.90 × IOVCC | — | IOVCC | 2, 3 |
| Input "Low" level voltage 2 RESETX pin | V _{IL2} | V | IOVCC=1.65V ~ 3.30V | -0.3 | — | 0.10 × IOVCC | 2, 3 |
| Output "High" level voltage 1 (DB[17:0], FMARK) | V _{OH} | V | IOVCC=1.65V ~ 3.30V, IOH=-0.1mA | 0.8 × IOVCC | — | — | 2 |
| Output "Low" level voltage 1 (DB[17:0], FMARK) | V _{OL} | V | IOVCC=1.65V ~ 3.30V, IOL=0.1mA | — | — | 0.20 × IOVCC | 2 |
| Input / Output leakage current | I _{LI} | μA | Vin=0 ~ IOVCC | -1 | — | 1 | 4 |
| Current Consumption ((IOVCC-GND) + (VCC-GND)) Normal operation mode (262,144-color display operation) | I _{OP1} | μA | fosc=600kHz (320-line drive), IOVCC=VCC=3.00V, fFLM=70Hz, Ta=25°C, frame memory data: 18'h000000 See below for other data. | — | 0.6 | 0.8 | 5 |
| Current Consumption ((IOVCC-GND) + (VCC-GND)) 8-color mode, 64-line partial display operation | I _{OP2} | μA | fosc=600kHz (64-line, partial display), IOVCC=VCC=3.00V, fFLM=40Hz, Ta=25°C, frame memory data: 18h'000000 See below for other data. | — | 140 | 350 | 5 |
| Current Consumption ((IOVCC-GND) + (VCC-GND)) Deep standby mode | I _{DST} | μA | IOVCC=VCC=3.00V, Ta=25°C | — | 0.1 | 1.0 | 5 |
| Current Consumption ((IOVCC-GND) + (VCC-GND)) Frame memory access mode | I _{RAM1} | mA | IOVCC=2.40V, VCC=3.00V, tCYCW=125ns, Ta=25°C, l80-8bit-I/F, TRIREG=1'h1, Consecutive frame memory access during display operation. | — | 2.6 | 3.2 | 5 |

Table 87 (VCC= 2.50V~3.30V, IOVCC=1.65V~3.30V, Ta=-40C~+85C) (See note 1) (Continued)

| | | | | | | | |
|---|---------------------|----|---|-----|-----|-----|---|
| LCD Power Supply Current (VCI-GND) 262,144-color display operation | Ici1 | mA | IOVCC=1.8V, VCC=VCI=2.8V, 320-line drive, fFLM=60Hz, Ta=25°C, Frame memory data: 18'h00000, REV=0, BC0=0, FP0=8, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h18, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h4, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) No load on the panel, COL=0 | — | 3.2 | 5.0 | 5 |
| LCD Power Supply Current (VCI-GND) 8-color (64-line partial) display operation | Ici2 | mA | IOVCC=1.8V, VCC=VCI=2.8V, 64-line partial display, fFLM=40Hz, Ta=25°C, Frame memory data: 18'h00000, REV=0, BC2=0, FP2=5, BP2=8, VC=3'h1, BT=3'h4, VRH=5'h18, VCM=7'h7F, VDV=5'h11, AP2=2'h3, DC02=3'h4, DC12=3'h2, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) No load on the panel, COL=1 | — | 0.8 | 1.5 | 5 |
| Output voltage dispersion | ΔV_O | mV | — | — | 5 | — | 6 |
| Average output voltage variance | ΔV_{Δ} | mV | — | -35 | — | 35 | 7 |

DC Characteristics 2

Table 88 DC Step-Up Circuit Characteristics

| Item | Unit | Test Condition | Min. | Typ. | Max. | Note | | |
|------------------------|-------|----------------|--|------|------|-------|------|---|
| Step-up Output Voltage | DDVDH | V | IOVCC=VCC=2.8V, VCI =2.8V, Ta=25°C, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h4, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, No load on the panel, Iload1= -3 [mA] | | 4.8 | 5.1 | - | - |
| | VGH | V | IOVCC=VCC=2.8V, VCI =2.8V, Ta=25°C, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h4, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload2=-100[uA], No load on the panel | | 14.4 | 15.1 | - | - |
| | VGL | V | IOVCC=VCC=2.8V, VCI =2.8V, Ta=25°C, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h4, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload3=+100[uA], No load on the panel | | - | -10.0 | -9.6 | - |
| | VCL | V | IOVCC=VCC=2.8V, VCI =2.8V, Ta=25°C, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h4, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload4=+200[uA], No load on the panel | | - | -2.55 | -2.4 | - |

Table 89 Internal Reference Voltage (VCC = 2.50V ~ 3.30V, Ta = 25°C)

| Item | Symbol | Unit | Min. | Typ. | Max. | Note |
|----------------------------|--------|------|------|------|------|------|
| Internal reference voltage | VCIR | V | - | 2.50 | - | 11 |

AC Characteristics

(VCC= 2.50V~3.30V, IOVCC=1.65V~3.30V, Ta=-40C~+85C) (See note 1)

Clock Characteristics

Table 90

| Item | Symbol | Unit | Test Condition | Min. | Typ. | Max. |
|----------------------------|--------|------|---------------------|------|------|------|
| Internal oscillation clock | fosc | kHz | IOVCC=VCC=3.0V 25°C | 558 | 600 | 642 |

80-System Bus Interface Timing Characteristics (18-/16-Bit Interface)

Table 91 (IOVCC=1.65V ~ 3.30V)

| Item | | Symbol | Unit | Timing Diagram | Min. | Typ. | Max. |
|------------------------------|------------------------------|--------------|------|----------------|------|------|------|
| Bus cycle time | Write | tCYCW | ns | Figure A | 75 | — | — |
| | Read | tCYCR | ns | Figure A | 600 | — | — |
| Write low-level pulse width | | PWLW | ns | Figure A | 40 | — | — |
| Read low-level pulse width | | PWLR | ns | Figure A | 400 | — | — |
| Write high-level pulse width | | PWHW | ns | Figure A | 25 | — | — |
| Read high-level pulse width | | PWHR | ns | Figure A | 200 | — | — |
| Write / Read rise/ fall time | | tWRr, WRf | ns | Figure A | — | — | 25 |
| Setup time | Write (RS to CSX, WRX) | tAS | ns | Figure A | 0 | — | — |
| | Read (RS to CSX, RDX) | | ns | Figure A | 10 | — | — |
| Address hold time | | tAH | ns | Figure A | 2 | — | — |
| Write data setup time | | tDSW | ns | Figure A | 25 | — | — |
| Write data hold time | | tH | ns | Figure A | 10 | — | — |
| Read data delay time | | tDDR | ns | Figure A | — | — | 300 |
| Read data hold time | | tDHR | ns | Figure A | 5 | — | — |

80-System Bus Interface Timing Characteristics (9-/8-Bit Interface)

Table 92 (IOVCC=1.65V ~ 3.30V)

| Item | | Symbol | Unit | Timing Diagram | Min. | Typ. | Max. |
|------------------------------|------------------------------|--------------|------|----------------|------|------|------|
| Bus cycle time | Write | tCYCW | ns | Figure A | 70 | — | — |
| | Read | tCYCR | ns | Figure A | 600 | — | — |
| Write low-level pulse width | | PWLW | ns | Figure A | 30 | — | — |
| Read low-level pulse width | | PWLR | ns | Figure A | 400 | — | — |
| Write high-level pulse width | | PWHW | ns | Figure A | 25 | — | — |
| Read high-level pulse width | | PWHR | ns | Figure A | 200 | — | — |
| Write / Read rise/ fall time | | tWRr, WRf | ns | Figure A | — | — | 25 |
| Setup time | Write (RS to CSX, WRX) | tAS | ns | Figure A | 0 | — | — |
| | Read (RS to CSX, RDX) | | ns | Figure A | 10 | — | — |
| Address hold time | | tAH | ns | Figure A | 2 | — | — |
| Write data setup time | | tDSW | ns | Figure A | 25 | — | — |
| Write data hold time | | tH | ns | Figure A | 10 | — | — |
| Read data delay time | | tDDR | ns | Figure A | — | — | 300 |
| Read data hold time | | tDHR | ns | Figure A | 5 | — | — |

Clock Synchronous Serial Interface Timing Characteristics

Table 93 (IOVCC=1.65V ~ 3.30V)

| Item | | Symbol | Unit | Timing Diagram | Min. | Typ. | Max. |
|-------------------------------|-----------------|------------|------|----------------|------|------|--------|
| Serial clock cycle time | Write (receive) | tSCYC | ns | Figure B | 100 | — | 20,000 |
| | Read (transmit) | tSCYC | ns | Figure B | 600 | — | 20,000 |
| Serial clock high-level width | Write (receive) | tSCH | ns | Figure B | 40 | — | — |
| | Read (transmit) | tSCH | ns | Figure B | 400 | — | — |
| Serial clock low-level width | Write (receive) | tSCL | ns | Figure B | 40 | — | — |
| | Read (transmit) | tSCL | ns | Figure B | 200 | — | — |
| Serial clock rise/fall time | | tScr, tScf | ns | Figure B | — | — | 20 |
| Chip select setup time | | tCSU | ns | Figure B | 20 | — | — |
| Chip select hold time | | tCH | ns | Figure B | 60 | — | — |
| Serial input data setup time | | tSISU | ns | Figure B | 30 | — | — |
| Serial input data hold time | | tSISH | ns | Figure B | 30 | — | — |
| Serial output data delay time | | tSOD | ns | Figure B | — | — | 130 |
| Serial output data hold time | | tSOH | ns | Figure B | 5 | — | — |

Reset Timing Characteristics

Table 94 (IOVCC = 1.65V ~ 3.30V)

| Item | | Symbol | Unit | Timing Diagram | Min. | Typ. | Max. |
|-----------------------|--|--------|------|----------------|------|------|------|
| Reset wait time | | trW | ms | Figure C-1 | 1 | — | — |
| Reset low-level width | | tRES | ms | Figure C-2 | 1 | — | — |
| Reset rise time | | trRES | μs | Figure C-2 | — | — | 10 |

RGB Interface Timing Characteristics

Table 95 18-/16-Bit RGB Interface (IOVCC=1.65V ~ 3.30V)

| Item | Symbol | Unit | Timing Diagram | Min. | Typ. | Max. |
|--|------------------|-------|----------------|------|------|------|
| VSYNC/HSYNC setup time | tSYNCS | clock | Figure D | 0.5 | — | 1.5 |
| ENABLE setup time | tENS | ns | Figure D | 10 | — | — |
| ENABLE hold time | tENH | ns | Figure D | 20 | — | — |
| DOTCLK low-level pulse width | PW _{DL} | ns | Figure D | 40 | — | — |
| DOTCLK high-level pulse width | PW _{DH} | ns | Figure D | 40 | — | — |
| DOTCLK cycle time | tCYCD | ns | Figure D | 100 | — | — |
| Data setup time | tPDS | ns | Figure D | 10 | — | — |
| Data hold time | tPDH | ns | Figure D | 40 | — | — |
| DOTCLK, VSYNC and HSYNC rise/fall time | trgbr, trgbf | ns | Figure D | — | — | 25 |

LCD Driver Output Characteristics

Table 96

| Item | Symbol | Unit | Test condition | Min. | Typ | Max | Note |
|---------------------------------|--------|------|--|------|-----|-----|------|
| Source driver output delay time | tdds | μs | <p>IOVCC=1.80V, VCC=VCI=2.80V, Ta=25°C, REV=0, BC0=0, FP0=5, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h1D, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h2, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2)</p> <p>Same change from same grayscale at all-time division source output pin.</p> <p>Time to reach ±35mV when VCOM polarity changes.</p> <p>Load resistance R=10kohm, Load capacitance C=20pF</p> | — | 25 | 30 | 9 |
| VCOM output delay time | tddv | μs | <p>IOVCC=1.80V, VCC=VCI=2.80V, Ta=25°C, REV=0, BC0=0, FP0=5, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h1D, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h2, SEPVCM=0</p> <p>Time to reach ±35mV when voltages on V0~V63 pins change.</p> <p>Load resistance R=100ohm, Load capacitance C=10nF</p> | — | 25 | 30 | 10 |

Notes on Electrical Characteristics

1. DC/AC electrical characteristics of bare die and wafer products are guaranteed at +85°C.
2. The followings illustrate the configurations of input, I/O, and output pins.

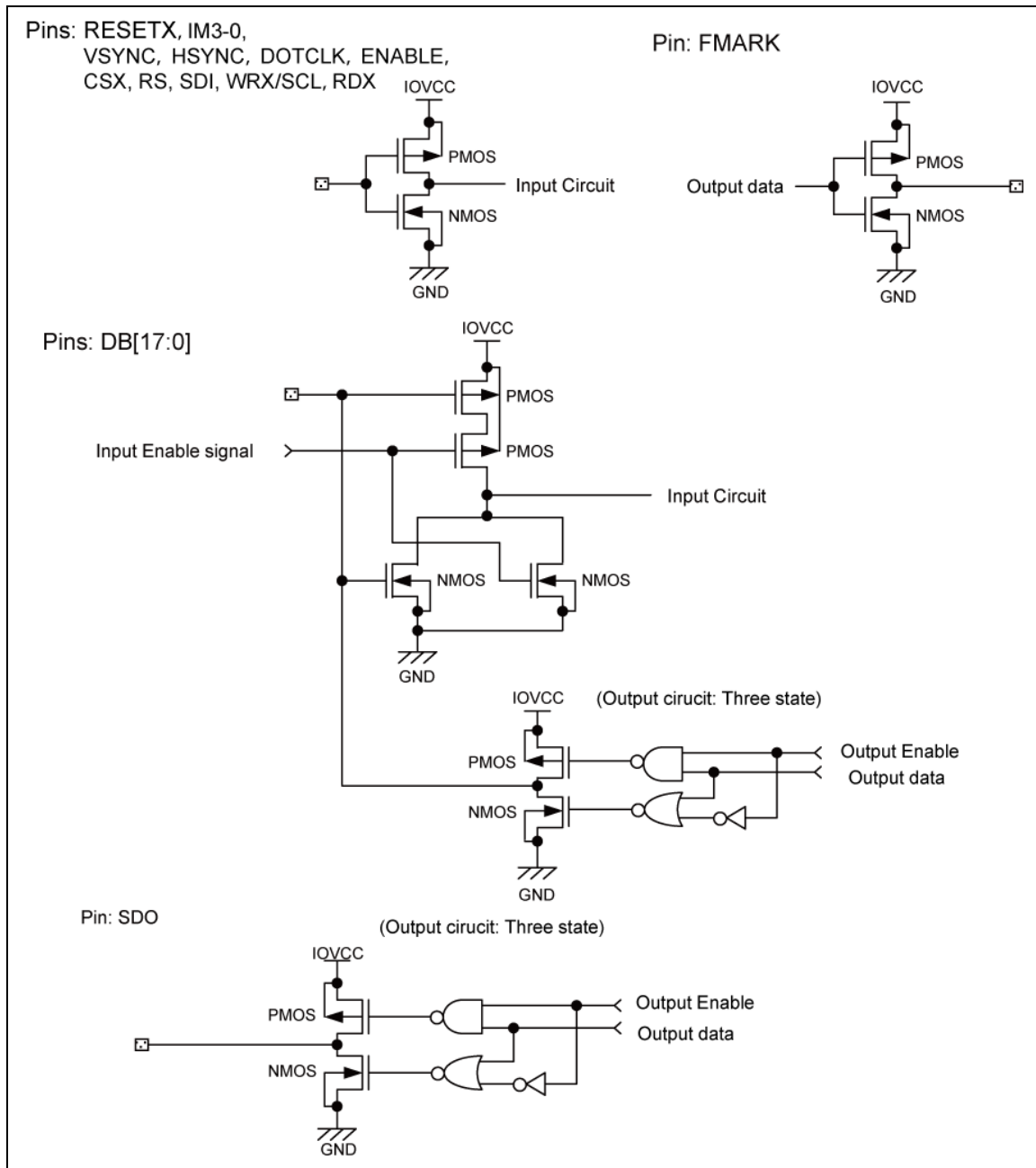


Figure 74

3. Fix pins as follows; TEST1 to TEST5 pins to GND, VDDTEST and VREFC pins to ground (AGND), and IM3/2/1/0 pins to IOVCC or ground (GND).
4. This excludes the current in the output-drive MOS.
5. This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is unaffected by whether the CSX pin is “high” or “low” while not accessing via interface pins.
6. The output voltage deviation is the difference in the voltages between output pins that are placed side by side in same display mode.
7. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for one chip with same display data.
8. This applies to internal oscillators when using an internal oscillator.
9. The liquid crystal driver output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line by checking the quality on the actual panel in use.
10. VCOM output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line checking the quality on the actual panel in use.
11. Internal reference voltage VCIR depends on temperature as shown in following graph.

Test Circuits

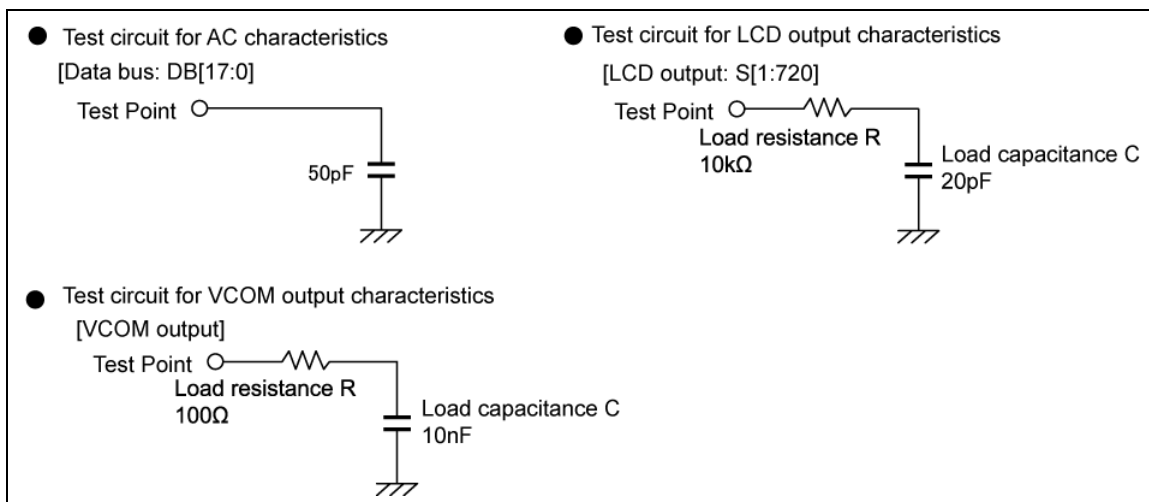


Figure 75

Timing Characteristics

80-System Bus Interface

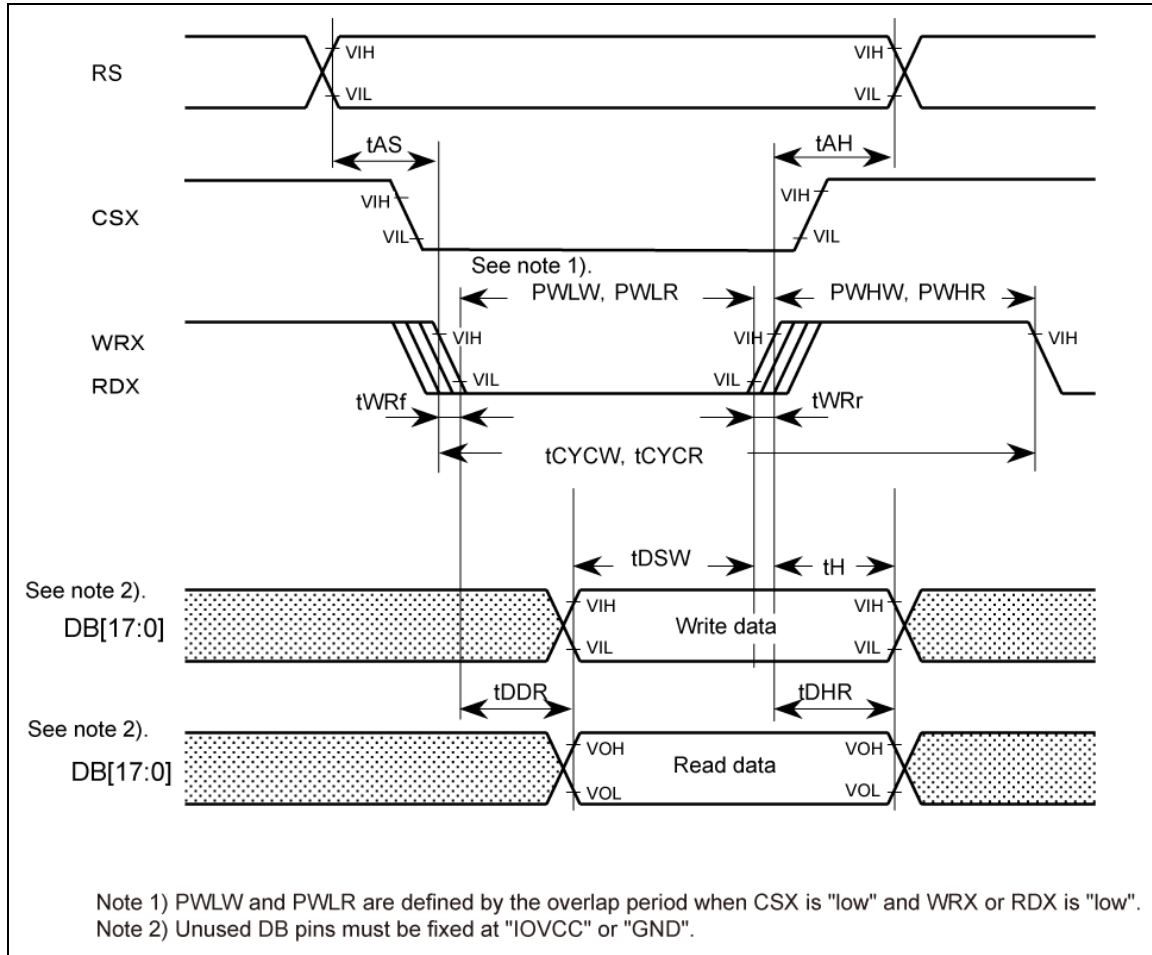


Figure A

Clock Synchronous Serial Interface

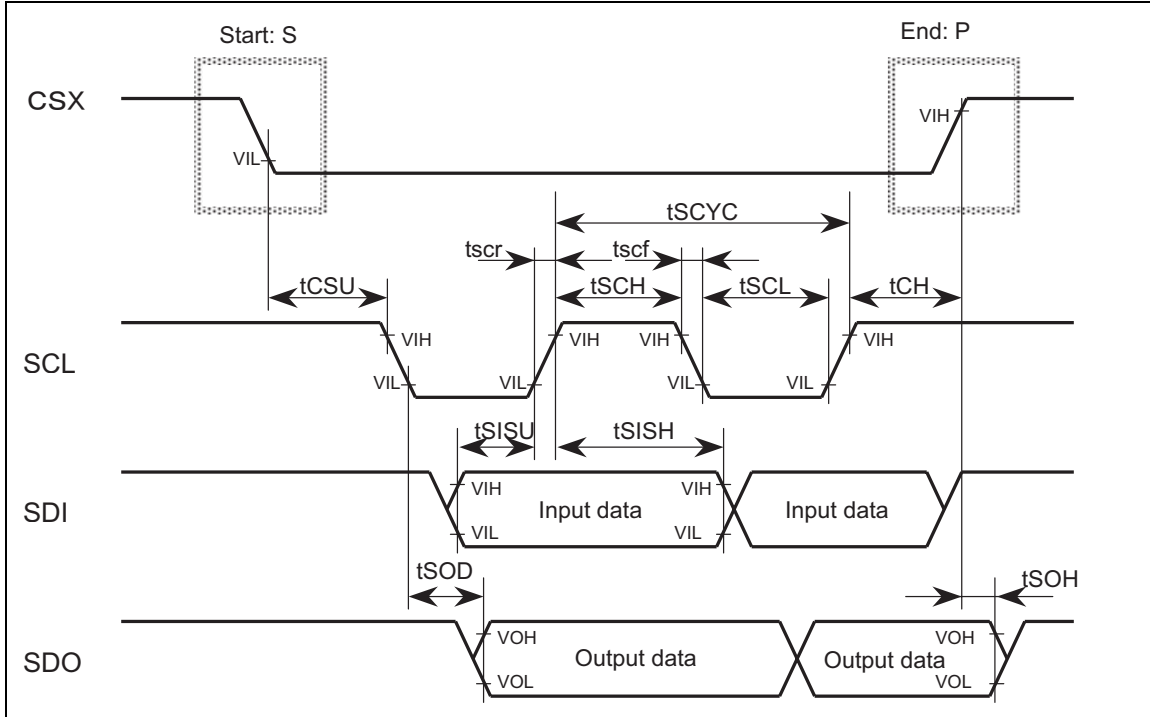
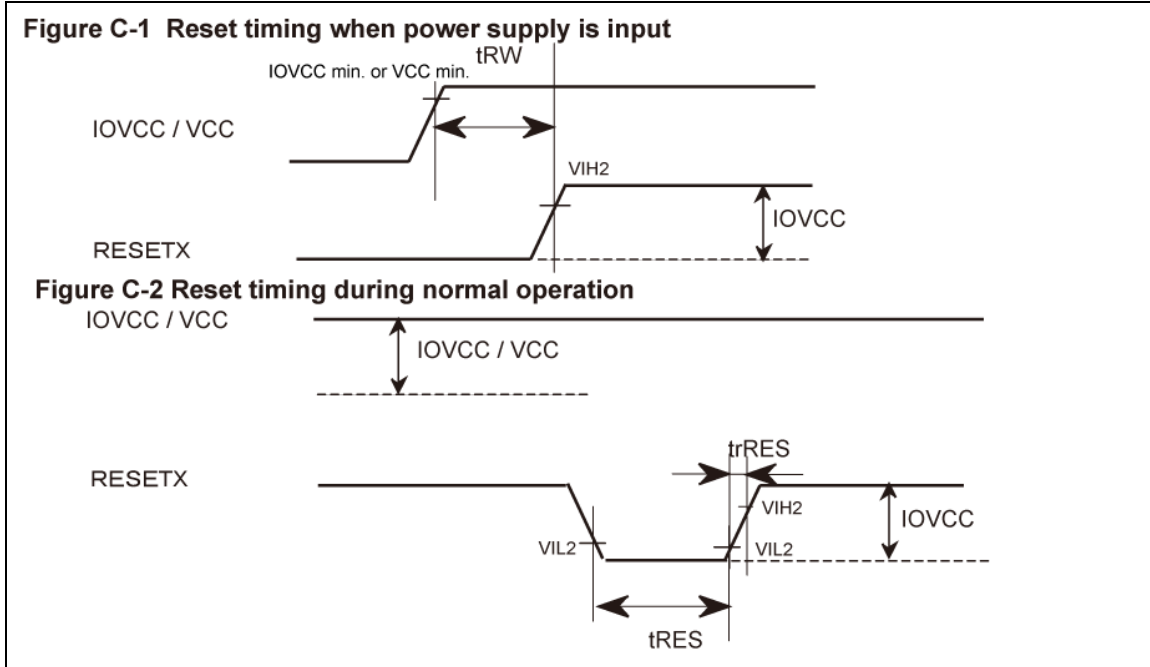


Figure B

Reset Operation



Figures C-1 and C-2

RGB Interface

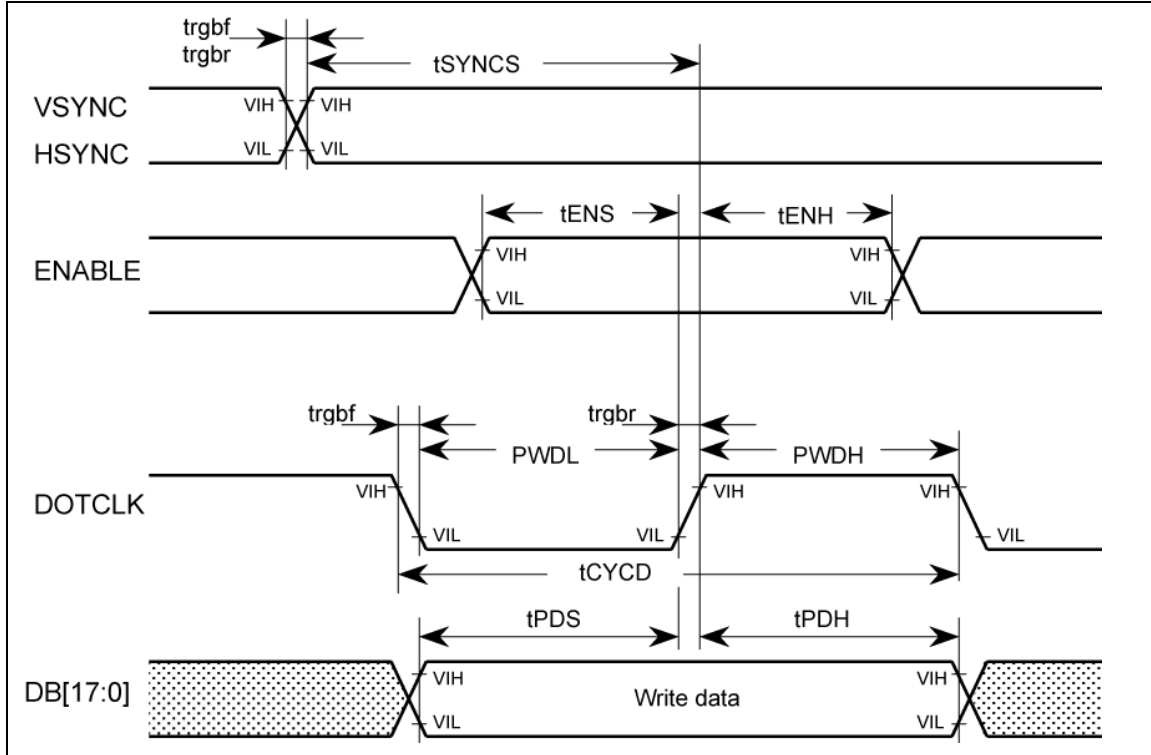


Figure D RGB Interface Timing

LCD Driver Output and VCOM Output

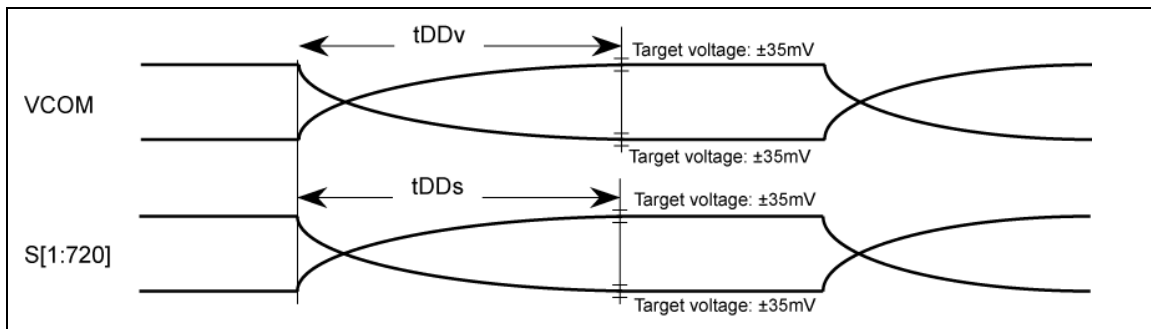


Figure E LCD Driver Output and VCOM Output

Revision Record

| Rev. | Date | Page No. | Contents of Modification | Drawn by | Approved by |
|---------|---|----------|--|----------|-------------|
| 0.01 | Jun. 11, 2008 | | First issue | | |
| 0.02 | Aug. 28, 2008 | 7 | 4 bits → 8 bits (user identification code). | | |
| | | 20 | Add "PAD Arrangement". | | |
| | | 21 | Change chip size and chip thickness, and delete "(T.B.D.)". | | |
| | | 22-35 | Add "PAD Coordinates". | | |
| | | 37 | Add "Wiring Example and Recommended Wiring Resistance". | | |
| | | 69 | UID[3:0] → UID[7:0]. | | |
| | | 84 | Change the default values of DIVE[1] and RTNE[0]. | | |
| | | 91 | UID1[3:0] → UID1[7:0]. | | |
| | | 92 | Delete the description of NVVRF, move the description of CALB from RA3h to RA4h, and add the description of VERIFLGER and VERIFLGWR. | | |
| | | 93 | Change the instruction list. | | |
| | | 151-152 | Change the circuits. | | |
| | | 157-158 | Change and add NVM sequences. | | |
| | | 162-164 | Change deep standby mode sequences. | | |
| | | 166 | Delete the specs of VPP1, VPP2, and VPP3A. | | |
| 169 | Change Typ. of IOP1, IOP2, and I _{RAM1} to (T.B.D.). | | | | |
| 0.03 | Dec. 3, 2008 | All | Change "RAM" and "GRAM" to "frame memory". | | |
| | | 10 | Add the description of NVAD bit assignment. | | |
| | | 38 | Delete "(may leave open)". (VPP1) | | |
| | | 92 | Delete NVAD[1] and change the NVDAT bit assignment and NVAD values in the table. | | |
| | | 93 | Change the bit assignment and add the description of the RTYRTL bits. | | |
| | | 94 | Delete NVAD[1] and add RTYRTL[3:0]. | | |
| | | 157 | Change the NVDAT bit assignment. | | |
| 158-159 | Add the note related to the RTYRTL bits. | | | | |
| 0.04 | Feb. 9, 2009 | 20 | Specs for VPP1 added. (Error correction) | | |
| | | 38 | SBD and notes on it deleted. | | |
| | | 49 | Note on the total of lines added. | | |
| | | 74 | Default value of NL[3] changed from 1 to 0. (Error correction) | | |
| | | 116 | Margin changed from ±10% to ±7%. (Error | | |

| Rev. | Date | Page No. | Contents of Modification | Drawn by | Approved by |
|------|---------------|---------------|---|----------|-------------|
| | | | correction) | | |
| | | 150-151 | Numbers of elements changed due to deleting SBD, and notes on it deleted. | | |
| | | 152 | Numbers of elements changed due to deleting SBD, and specs of SBD deleted. | | |
| | | 166 | I _{OP1} (Typ.) changed from (T.B.D.) to 0.6, I _{OP2} (Typ.) changed from (T.B.D.) to 140, and I _{RAM1} (Typ.) changed from (T.B.D.) to 2.6. (Error correction) | | |
| | | 167 | Specs for NVM operating current deleted. (Error correction) | | |
| 1.00 | Mar. 11, 2009 | 21, 23-36, 38 | Rev. no. changed to 1.00. (Fixed) | | |
| | | 156 | Sequence of and note on gate off command added, RA1h changed from 16'h00** to 16'hFF** and EOP changed from 2'h3 to 2'h1. | | |
| | | 157 | Sequence of and note on gate off command added. | | |
| | | 166 | "T.B.D." deleted from the title, and (Max.) of I _{OP1} , I _{OP2} , I _{DST} , and I _{RAM1} defined. | | |
| | | 167 | "T.B.D." deleted from the title, and (Max.) of I _{CI1} and I _{CI2} defined. | | |
| | | 168, 172 | "T.B.D." deleted from the titles. | | |
| | | 169-171 | "T.B.D." in the titles and note about target value deleted. | | |
| | | 173 | "T.B.D." deleted from the title, and (Max.) of tdds and tddv defined. | | |

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Notes:

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